High-Voltage Direct-Current Transmission

High-voltage direct-current (HVDC) transmission has advantages over ac transmission in special situations. The first commercial application of HVDC transmission was between the Swedish mainland and the island of Gotland in 1954. This system used mercury-arc valves and provided a 20 MW underwater link of 90 km. Since then, there has been a steady increase in the application of HVDC transmission.

With the advent of thyristor valve converters, HVDC transmission became even more attractive. The first HVDC system using thyristor valves was the Eel River scheme commissioned in 1972, forming a 320 MW back-to-back dc interconnection between the power systems of the Canadian provinces of New Brunswick and Quebec. Thyristor valves have now become standard equipment for dc converter stations. Recent developments in conversion equipment have reduced their size and cost, and improved their reliability. These developments have resulted in a more widespread use of HVDC transmission. In North America, the total capacity of HVDC links in 1987 was over 14,000 MW [1]. There are more links under construction.

The following are the types of applications for which HVDC transmission has been used:

1. Underwater cables longer than about 30 km. AC transmission is impractical for such distances because of the high capacitance of the cable requiring intermediate compensation stations.

2. Asynchronous link between two ac systems where ac ties would not be feasible because of system stability problems or a difference in nominal frequencies of the two systems.

3. Transmission of large amounts of power over long distances by overhead lines. HVDC transmission is a competitive alternative to ac transmission for distances in excess of about 600 km.

HVDC systems have the ability to rapidly control the transmitted power. Therefore, they have a significant impact on the stability of the associated ac power systems. An understanding of the characteristics of the HVDC systems is essential for the study of the stability of the power system. More importantly, proper design of the HVDC controls is essential to ensure satisfactory performance of the overall ac/dc system.

This chapter will provide a general introduction to the basic principles of operation and control of HVDC systems and describe their modelling for power-flow and stability studies. Two terminal systems will be considered in detail, followed by a brief discussion of multiterminal systems.

For additional general information on HVDC transmission, the reader may refer to references 2 to 8. Reference 9 provides information related to specification of HVDC systems.

10.1 HVDC SYSTEM CONFIGURATIONS AND COMPONENTS

10.1.1 Classification of HVDC Links

HVDC links may be broadly classified into the following categories:

- Monopolar links
- Bipolar links
- Homopolar links

The basic configuration of a *monopolar link* is shown in Figure 10.1. It uses one conductor, usually of negative polarity. The return path is provided by ground or water. Cost considerations often lead to the use of such systems, particularly for cable transmission. This type of configuration may also be the first stage in the development of a bipolar system.

Instead of ground return, a metallic return may be used in situations where the earth resistivity is too high or possible interference with underground/underwater metallic structures is objectionable. The conductor forming the metallic return is at low voltage.

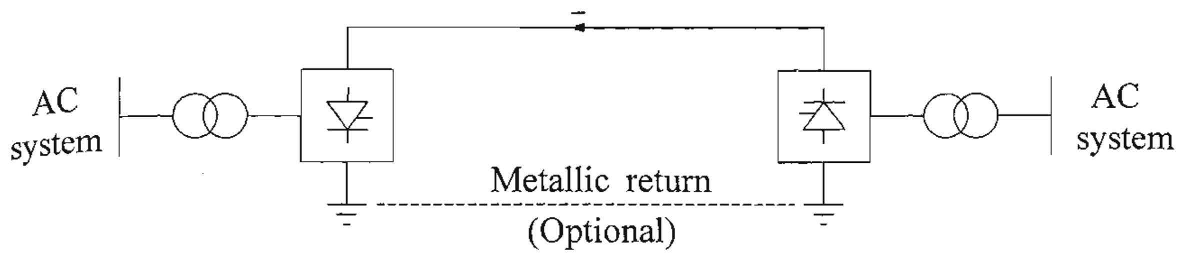


Figure 10.1 Monopolar HVDC link

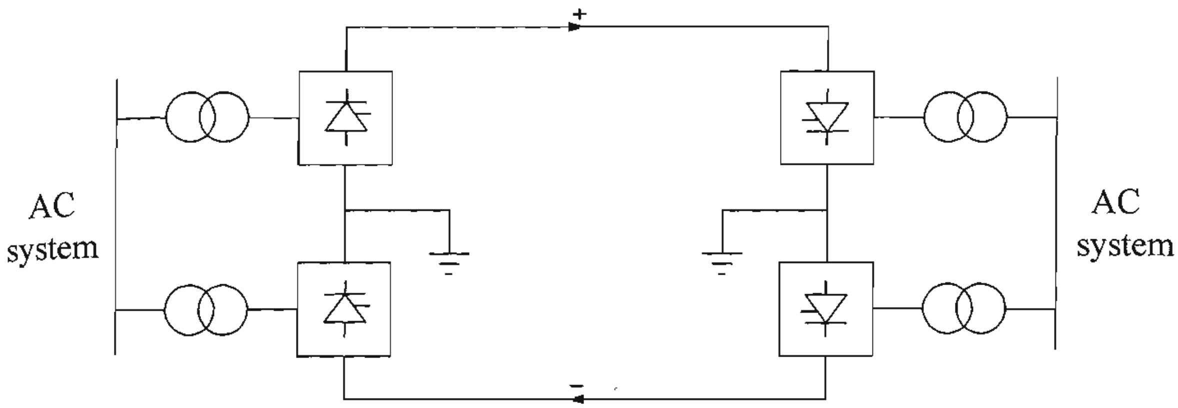


Figure 10.2 Bipolar HVDC link

The *bipolar link* configuration is shown in Figure 10.2. It has two conductors, one positive and the other negative. Each terminal has two converters of equal rated voltage, connected in series on the dc side. The junctions between the converters is grounded. Normally, the currents in the two poles are equal, and there is no ground current. The two poles can operate independently. If one pole is isolated due to a fault on its conductor, the other pole can operate with ground and thus carry half the rated load or more by using the overload capabilities of its converters and line.

From the viewpoint of lightning performance, a bipolar HVDC line is considered to be effectively equivalent to a double-circuit ac transmission line. Under normal operation, it will cause considerably less harmonic interference on nearby facilities than the monopolar system. Reversal of power-flow direction is achieved by changing the polarities of the two poles through controls (no mechanical switching is required).

In situations where ground currents are not tolerable or when a ground electrode is not feasible for reasons such as high earth resistivity, a third conductor is used as a metallic neutral. It serves as the return path when one pole is out of service or when there is imbalance during bipolar operation. The third conductor requires low insulation and may also serve as a shield wire for overhead lines. If it is fully insulated, it can serve as a spare.

The *homopolar link*, whose configuration is shown in Figure 10.3, has two or more conductors, all having the same polarity. Usually a negative polarity is preferred because it causes less radio interference due to corona. The return path for such a system is through ground. When there is a fault on one conductor, the entire converter is available for feeding the remaining conductor(s) which, having some overload capability, can carry more than the normal power. In contrast, for a bipolar scheme reconnection of the whole converter to one pole of the line is more complicated and usually not feasible. Homopolar configuration offers an advantage in this regard in situations where continuous ground current is acceptable.

The ground current can have side effects on gas or oil pipe lines that lie within a few miles of the system electrodes. Pipelines act as conductors for the ground current which can cause corrosion of the metal. Therefore, configurations using ground return may not always be acceptable.

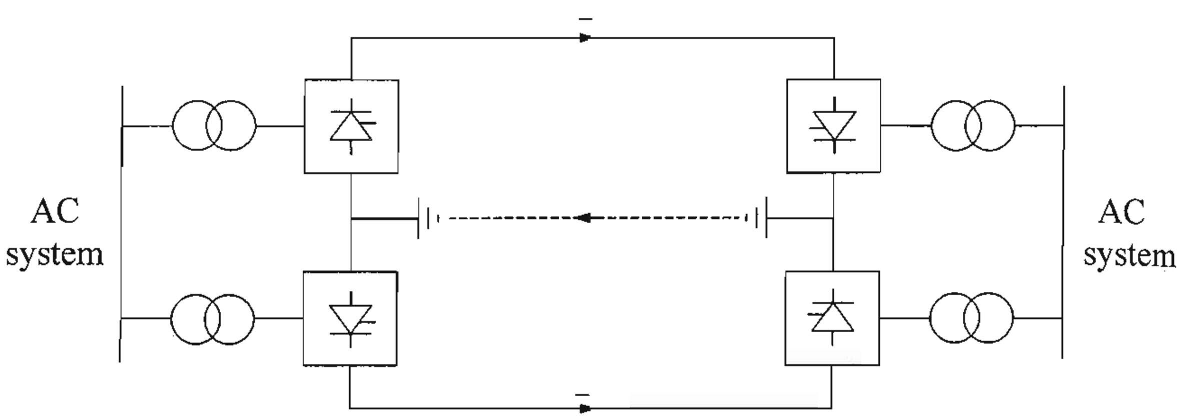


Figure 10.3 Homopolar HVDC link

Each of the above HVDC system configurations usually has cascaded groups of several converters, each having a transformer bank and a group of valves. The converters are connected in parallel on the ac side (transformer) and in series on the dc side (valve) to give the desired level of voltage from pole to ground.

Back-to-back HVDC systems (used for asynchronous ties) may be designed for monopolar or bipolar operation with a different number of valve groups per pole, depending on the purpose of the interconnection and the desired reliability.

Most point-to-point (two-terminal) HVDC links involving lines are bipolar, with monopolar operation used only during contingencies. They are normally designed to provide maximum independence between poles to avoid bipolar shutdowns.

A multiterminal HVDC system is formed when the dc system is to be connected to more than two nodes on the ac network. The possible configurations of multiterminal systems will be discussed in Section 10.8.

10.1.2 Components of HVDC Transmission System

The main components associated with an HVDC system are shown in Figure 10.4, using a bipolar system as an example. The components for other configurations are essentially the same as those shown in the figure. The following is a brief description of each component.

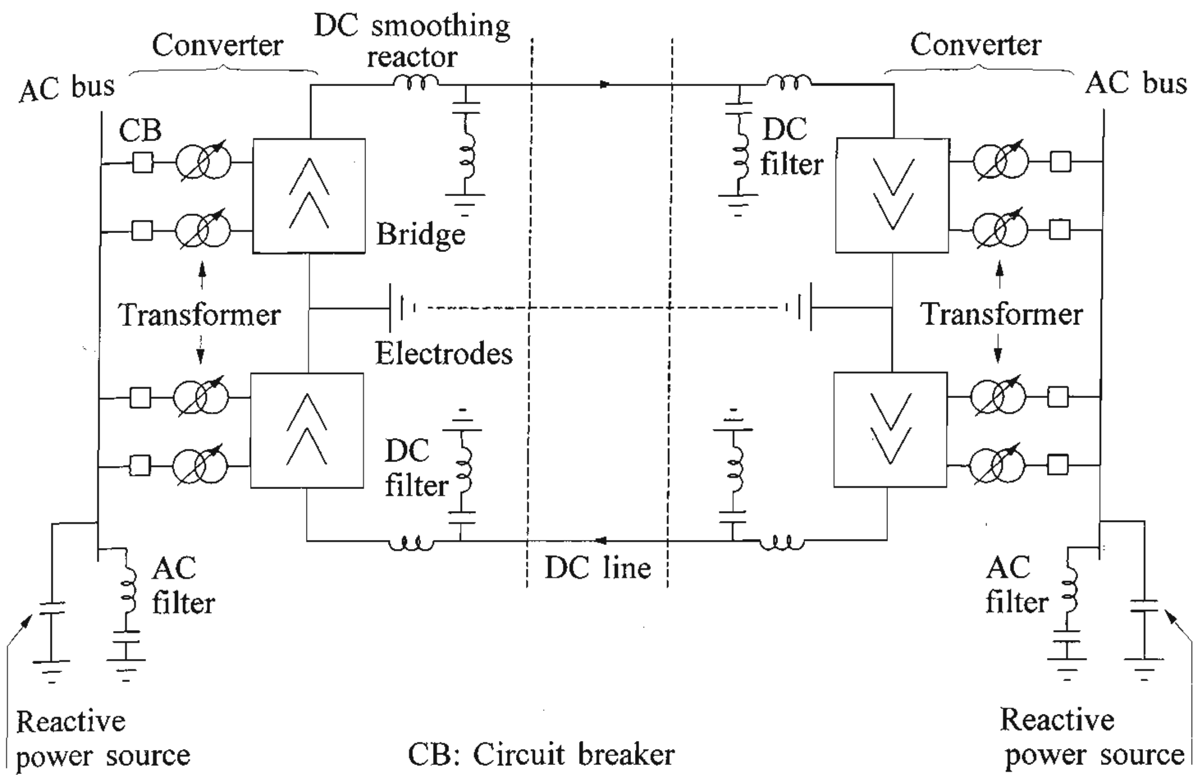


Figure 10.4 A schematic of a bipolar HVDC system identifying main components

Converters. They perform ac/dc and dc/ac conversion, and consist of valve bridges and transformers with tap changers. The valve bridges consist of high-voltage valves connected in a 6-pulse or 12-pulse arrangement as described in Section 10.2. The converter transformers provide ungrounded three-phase voltage source of appropriate level to the valve bridge. With the valve side of the transformer ungrounded, the dc system will be able to establish its own reference to ground, usually by grounding the positive or negative end of the valve converter.

Smoothing Reactors. These are large reactors having inductance as high as 1.0 H connected in series with each pole of each converter station. They serve the following purposes:

- Decrease harmonic voltages and currents in the dc line.
- Prevent commutation failure in inverters.
- Prevent current from being discontinuous at light load.
- Limit the crest current in the rectifier during short-circuit on the dc line.

Harmonic Filters. Converters generate harmonic voltages and currents on both ac and dc sides. These harmonics may cause overheating of capacitors and nearby generators, and interference with telecommunication systems. Filters are therefore used on both ac and dc sides.

Reactive Power Supplies. As we will see in Section 10.2, dc converters inherently absorb reactive power. Under steady-state conditions, the reactive power consumed is about 50% of active power transferred. Under transient conditions, the consumption of reactive power may be much higher. Reactive power sources are therefore provided near the converters. For strong ac systems, these are usually in the form of shunt capacitors. Depending on the demands placed on the dc link and on the ac system, part of the reactive power source may be in the form of synchronous condensers or static var compensators. The capacitors associated with the ac filters also provide part of the reactive power required.

Electrodes. Most dc links are designed to use earth as a neutral conductor for at least brief periods of time. The connection to the earth requires a large-surface-area conductor to minimize current densities and surface voltage gradients. This conductor is referred to as an electrode. As discussed earlier, if it is necessary to restrict the current flow through the earth, a metallic return conductor may be provided as part of the dc line.

DC Lines. They may be overhead lines or cables. Except for the number of conductors and spacing required, dc lines are very similar to ac lines.

AC Circuit Breakers. For clearing faults in the transformer and for taking the dc link out of service, circuit-breakers are used on the ac side. They are not used for clearing dc faults, since these faults can be cleared more rapidly by converter control.

10.2 CONVERTER THEORY AND PERFORMANCE EQUATIONS

A converter performs ac/dc conversion and provides a means of controlling the power flow through the HVDC link. The major elements of the converter are the valve bridge and converter transformer. The valve bridge is an array of high-voltage switches or valves that sequentially connect the three-phase alternating voltage to the dc terminals so that the desired conversion and control of power are achieved. The converter transformer provides the appropriate interface between the ac and dc systems.

In this section, we will describe the structure and operation of practical converter circuits. In addition, we will develop equations relating dc quantities and fundamental frequency ac quantities.

10.2.1 Valve Characteristics

The valve in an HVDC converter is a controlled electronic switch. It normally conducts in only one direction, the forward direction, from anode to cathode. When it is conducting, there is only a small voltage drop across it. In the reverse direction, when the voltage applied across the valve is such that the cathode is positive relative to the anode, the valve blocks the current.

The early HVDC systems used mercury-arc valves. Mercury-arc valves with rated currents of the order of 1,000 to 2,000 A and rated peak inverse voltage of 50 to 150 kV have been built and used. Among the disadvantages of mercury-arc valves are their large size and tendency to conduct in the reverse direction.

All HVDC systems built since the mid-1970s have used thyristor valves. Thyristor valves rated at 2,500 to 3,000 A and 3 to 5 kV have been developed. The thyristors are connected in series to achieve the desired system voltage. They are available in various designs: air cooled, air insulated; oil cooled, oil insulated; water cooled, air insulated; and freon cooled, SF_6 insulated. The valves can be designed for indoor or outdoor installation.

For the valve to conduct, it is necessary for the anode to be positive relative to the cathode. In a mercury-arc valve, with the control grid at sufficiently negative voltage with respect to the cathode, the valve is prevented from conducting, although the anode may be positive. The instant of firing can be controlled by the grid.

Similarly, a thyristor valve will conduct only when the anode is positive with respect to the cathode and when there is a positive voltage applied to the gate. Conduction may be initiated by applying a momentary or sustained current pulse of proper polarity to the gate.

Once conduction is initiated, the current through the valve continues until current drops to zero and a reverse voltage bias appears across the valve. In the forward direction, the current is blocked until a control pulse is applied to the gate. When not conducting, the valve should be capable of withstanding the forward or reverse bias voltages appearing between its cathode and anode.

Figure 10.5 shows the symbol used to represent a controlled valve (mercury-arc or thyristor).

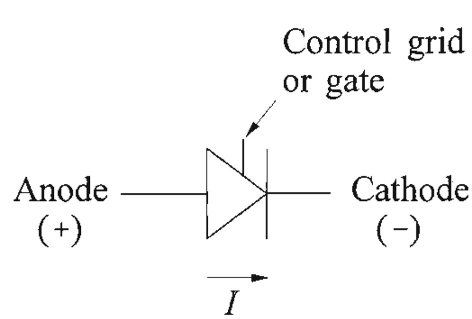


Figure 10.5 Symbol for controlled valve

10.2.2 Converter Circuits

The basic module of an HVDC converter is the three-phase, full-wave bridge circuit shown in Figure 10.6. This circuit is also known as a Graetz bridge. Although there are several alternative configurations possible, the Graetz bridge has been universally used for HVDC converters as it provides better utilization of the converter transformer and a lower voltage across the valve when not conducting [2,6]. The latter is referred to as the peak inverse voltage and is an important factor that determines the rating of the valves.

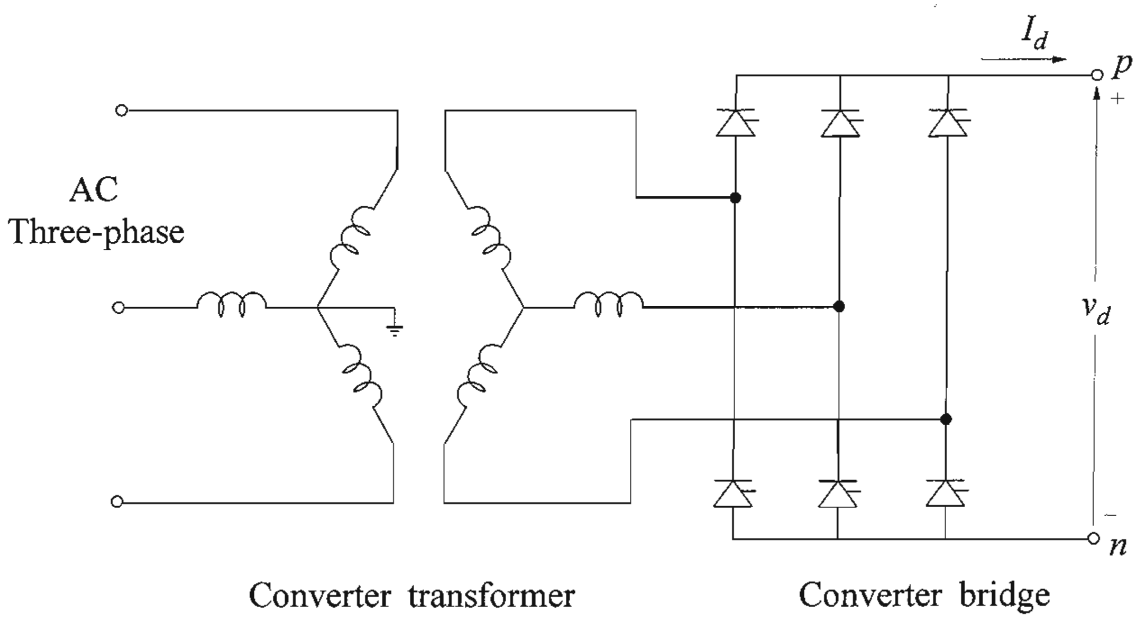


Figure 10.6 Three-phase, full-wave bridge circuit

The converter transformer has on-load taps on the ac side for voltage control. The ac side windings of the transformer are usually star-connected with grounded neutral; the valve side-windings are delta-connected or star-connected with ungrounded neutral.

Analysis of three-phase, full-wave bridge circuit

For purposes of analysis, we will make the following assumptions:

(a) The ac system, including the converter transformer, may be represented by an ideal source of constant voltage and frequency in series with a lossless inductance (representing primarily the transformer leakage inductance).

(b) The direct current (I_d) is constant and ripple-free; this is justified because of the large smoothing reactor (L_d) used on the dc side.

(c) The valves are ideal switches with zero resistance when conducting, and infinite resistance when not conducting.

Based on the above assumptions, the bridge converter of Figure 10.6 may be represented by the equivalent circuit shown in Figure 10.7.

Let the instantaneous line-to-neutral source voltages be

$$\begin{aligned} e_a &= E_m \cos(\omega t + 60°) \\ e_b &= E_m \cos(\omega t - 60°) \\ e_c &= E_m \cos(\omega t - 180°) \end{aligned} \tag{10.1}$$

The line-to-line voltages are then

$$\begin{aligned} e_{ac} &= e_a - e_c = \sqrt{3} E_m \cos(\omega t + 30°) \\ e_{ba} &= e_b - e_a = \sqrt{3} E_m \cos(\omega t - 90°) \\ e_{cb} &= e_c - e_b = \sqrt{3} E_m \cos(\omega t + 150°) \end{aligned} \tag{10.2}$$

Figure 10.8(a) shows the voltage waveforms corresponding to Equations 10.1 and 10.2.

To simplify analysis and help understand the operation of the bridge converter, we will first consider the case with negligible source inductance (i.e., L_c=0) and no ignition delay. After developing a basic understanding of the converter performance, we will extend the analysis to include the effect of delaying the valve ignition through gate/grid control and then the effect of source inductance.

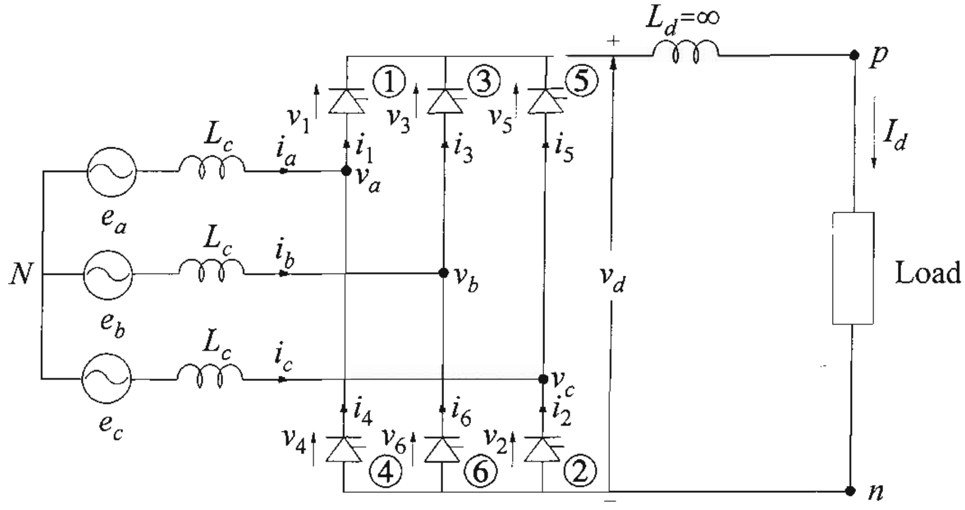
Analysis assuming negligible source inductance

(a) With no ignition delay

In Figure 10.7, the cathodes of valves 1, 3, and 5 of the upper row are connected together. Therefore, when the phase-to-neutral voltage of phase a is more positive than the voltages of the other two phases, valve 1 conducts. The common potential of the cathodes of the three valves is then equal to that of the anode of valve 1. Since the cathodes of valves 3 and 5 are at a higher potential than their anodes, these valves do not conduct.

In the lower row, the anodes of valves 2, 4 and 6 are connected together. Therefore, valve 2 conducts when phase c voltage is more negative than the other two phases.

From the waveforms shown in Figure 10.8(a) we see that valve 1 conducts when ωt is between $-120°$ and $0°$, since e_a is greater than e_b or e_c. Valve 2 conducts when ωt is between $-60°$ and $60°$, since e_c is more negative than e_a or e_b during this



Note: Valves are numbered in order of firing.

Figure 10.7 Equivalent circuit for three-phase full-wave bridge converter

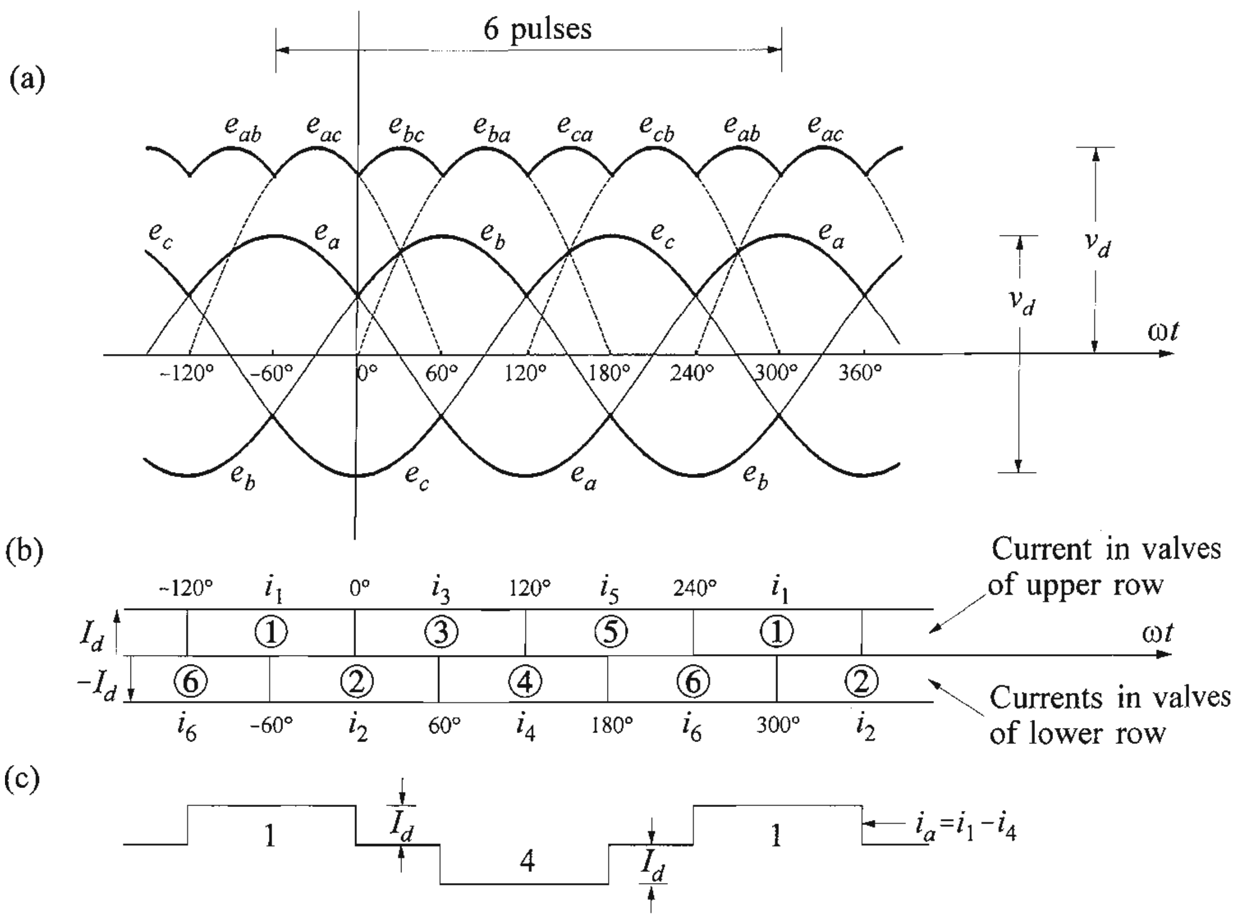


Figure 10.8 Waveforms of voltages and currents of bridge circuit of Figure 10.7
(a) Source line-to-neutral and line-to-line voltages
(b) Valve currents and periods of conduction
(c) Phase current i_a

period. This is shown in Figure 10.8(b), which identifies the period of conduction of each valve, and the magnitude and duration of current in it. Since, by assumption, the direct current I_d is assumed constant, the current in each valve is I_d when conducting and zero when not conducting.

Let us now examine the period when ωt is between 0° and 120°. Just before ωt=0, valves 1 and 2 are conducting. Just after ωt=0°, e_b becomes more positive than e_a and valve 3 ignites; valve 1 is extinguished because its cathode is now at a higher potential than its anode. For the next 60°, valves 2 and 3 conduct. At ωt=60°, e_a is more negative than e_c, causing valve 4 to ignite and valve 2 to extinguish.

At ωt=120°, e_c is more positive than e_b, resulting in the ignition of valve 5 and extinction of valve 3. Similarly, at ωt=180° conduction switches from valve 4 to 6 in the lower row; at ωt=240° conduction switches from valve 5 to valve 1 in the upper row. This completes one cycle, and the sequence continues.

The valve-switching sequence is illustrated in Figure 10.9, which shows only the conducting valves during the six distinct periods of a complete cycle.

Each valve thus conducts for a period of 120°. When it is conducting, the magnitude of valve current is I_d; the valves in the upper row carry positive current and the valves in the lower row carry negative (or return) current.

The current in each phase of the ac source is composed of currents in the two valves connected to that phase. For example, the current in phase a, as shown in Figure 10.8(c), is equal to $i_1 - i_4$. This represents the current in the secondary (valve side) winding of the converter transformer of Figure 10.6.

The transfer of current from one valve to another in the same row is called "commutation." In the above analysis, we have assumed that the source inductance L_c is negligible. Therefore, commutation occurs instantaneously, i.e., without "overlap." The result is that no more than two valves (one from the top row and the other from the bottom row) conduct at any time.

From Figure 10.8(a), we see that the number of pulsations (cycles of ripple) of v_d per cycle of alternating voltage is six. Hence, the bridge circuit of Figure 10.6 is referred to as a "6-pulse bridge circuit."

Average direct voltage:

The instantaneous direct voltage v_d across the bridge (between the cathodes of the upper-row valves and anodes of lower-row valves) is composed of 60° segments of the line-to-line voltages. Therefore, the average direct voltage can be found by integrating the instantaneous values over any 60° period.

Denoting ωt by θ, and considering the period between ωt=−60° and 0°, the average direct voltage with no ignition delay is given by

$$V_{d0} = \frac{3}{\pi} \int_{-60^\circ}^{0} e_{ac}\, d\theta$$

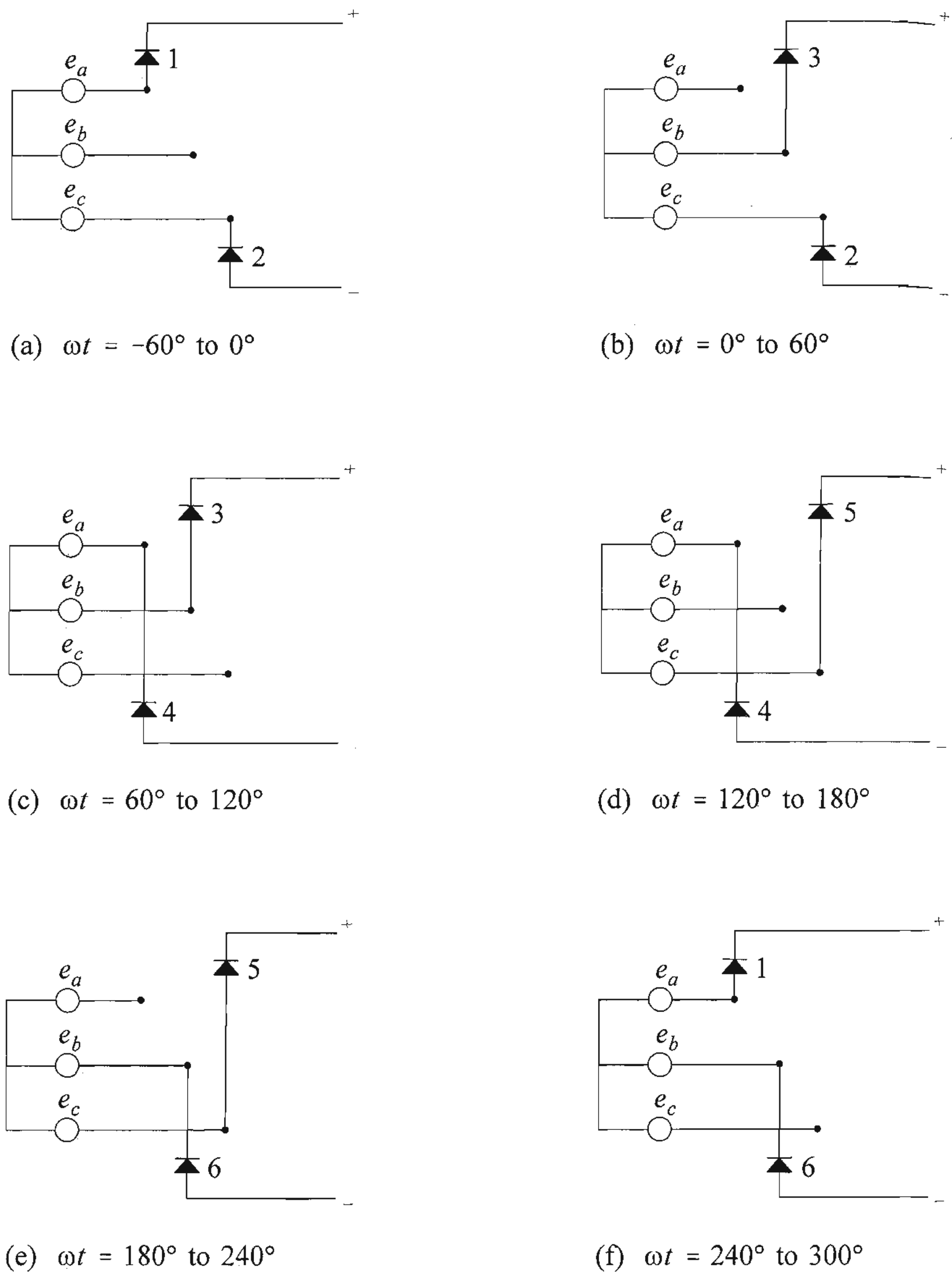


Figure 10.9 Valve-switching sequence with no ignition delay and no overlap

Substituting for e_{ac} from Equation 10.2, we get

$$V_{d0} = \frac{3}{\pi}\int_{-60°}^{0} \sqrt{3}E_m \cos(\theta + 30°)\, d\theta$$

$$= \frac{3\sqrt{3}}{\pi}E_m \sin(\theta + 30°)\Big|_{-60°}^{0} \qquad (10.3A)$$

$$= \frac{3\sqrt{3}}{\pi}E_m 2\sin 30° = \frac{3\sqrt{3}}{\pi}E_m = 1.65E_m$$

where E_m is the peak value of the line-to-neutral voltage.

In terms of RMS line-to-neutral (E_{LN}) and line-to-line (E_{LL}) voltages, the expression for V_{d0} becomes

$$V_{d0} = \frac{3\sqrt{6}}{\pi}E_{LN} = 2.34\,E_{LN} \qquad (10.3B)$$

$$= \frac{3\sqrt{2}}{\pi}E_{LL} = 1.35\,E_{LL} \qquad (10.3C)$$

and V_{d0} is called the "ideal no-load direct voltage."

(b) With ignition delay

The grid or gate control can be used to delay the ignition of the valves. The "delay angle" is denoted by α; it corresponds to time delay of α/ω seconds.

With delay, valve 3 ignites when $\omega t = \alpha$ (instead of $\omega t = 0$), valve 4 when $\omega t = \alpha + 60°$, valve 5 when $\omega t = \alpha + 120°$, and so on. This is illustrated in Figure 10.10.

The delay angle is limited to 180°. If α exceeds 180°, the valve fails to ignite. For example, consider the ignition of valve 3. With $\alpha = 0$, valve 3 ignites at $\omega t = 0$. The ignition can be delayed up to $\omega t = 180°$. Beyond this, e_b is no longer greater than e_a, and hence valve 3 will not ignite.

Average direct voltage:

Referring to Figure 10.10, the average direct voltage V_d when the delay angle is equal to α is given by

$$V_d = \frac{3}{\pi}\int_{-(60°-\alpha)}^{\alpha} e_{ac}\, d\theta = \frac{3}{\pi}\int_{\alpha-60°}^{\alpha} \sqrt{3}E_m \cos(\theta + 30°)\, d\theta$$

$$= V_{d0}\int_{\alpha-60°}^{\alpha} \cos(\theta + 30°)\, d\theta = V_{d0}\sin(\theta + 30°)\Big|_{\alpha-60°}^{\alpha} \qquad (10.4)$$

$$= V_{d0}[\sin(\alpha + 30°) - \sin(\alpha - 30°)]$$

$$= V_{d0}(2\sin 30°)\cos\alpha = V_{d0}\cos\alpha$$

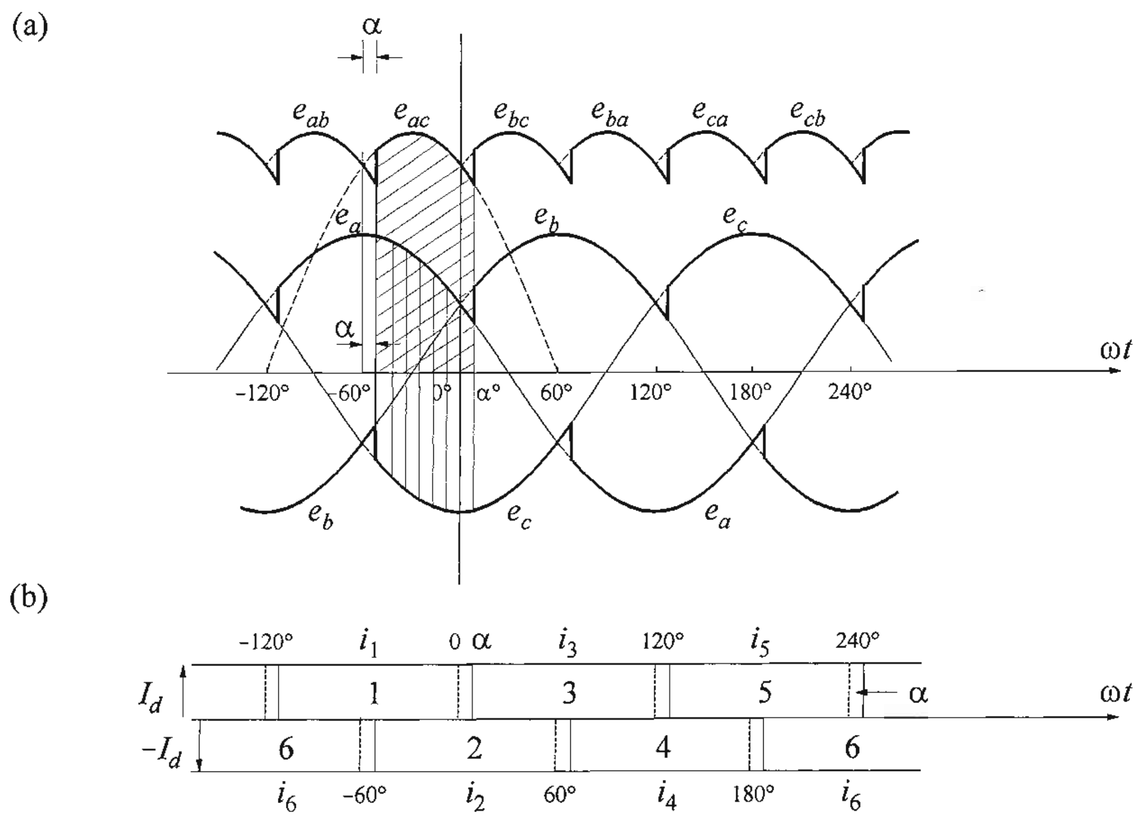


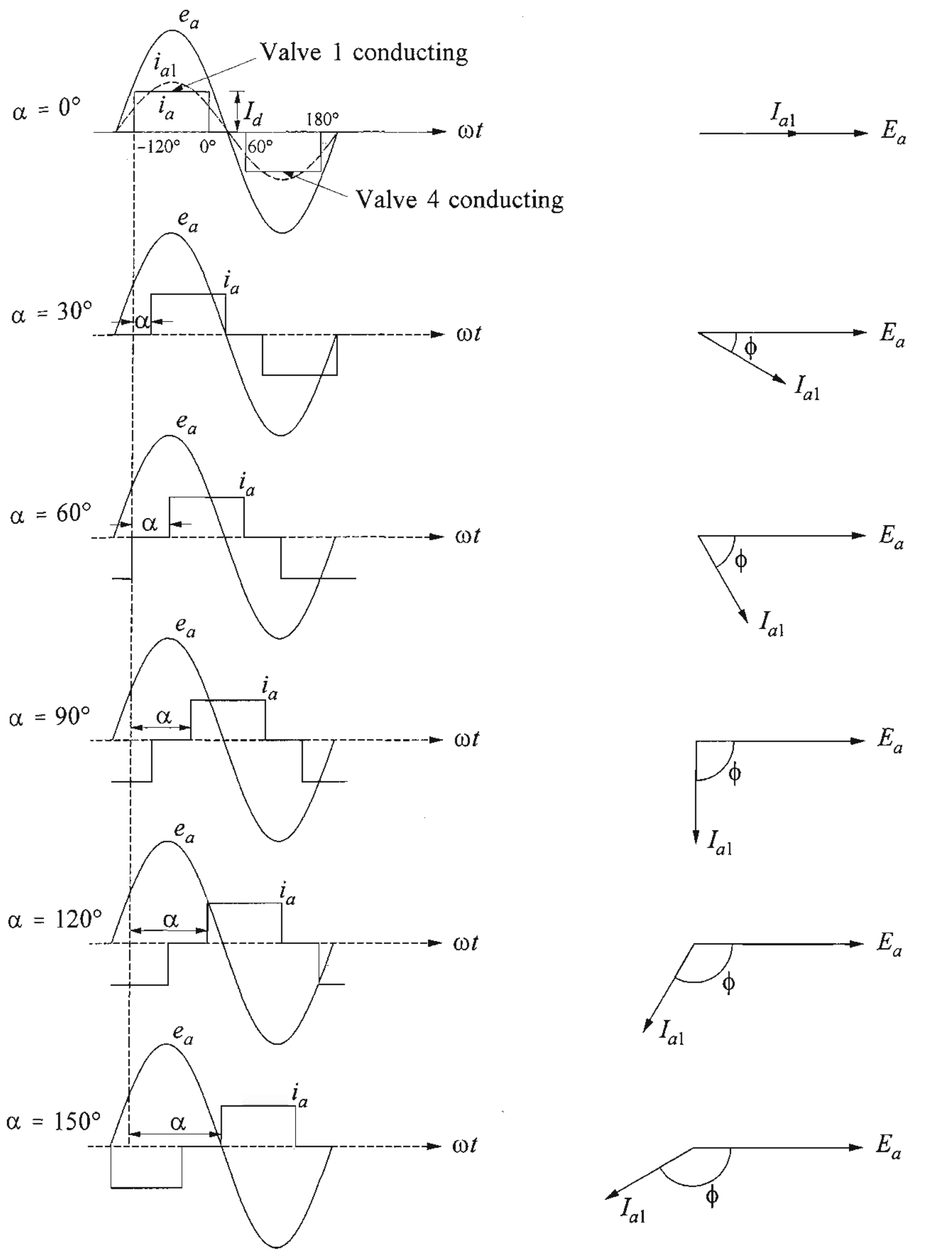
Figure 10.10 Voltage waveforms and valve currents, with ignition delay

The effect of the delayed ignition is thus to reduce the average direct voltage by the factor $\cos\alpha$.

Since α can range from 0° to 180°, $\cos\alpha$ can range from 1 to −1. Therefore, V_d can range from V_{d0} to $-V_{d0}$. Negative V_d, as discussed later in this section, represents inversion as opposed to rectification.

Current and phase relations:

As the ignition delay angle α is increased, the phase displacement between alternating voltage and alternating current in a supply phase also changes. This is illustrated in Figure 10.11 for phase *a*. The current wave shape, as shown in Figure 10.8(c), is composed of rectangular segments associated with currents in valves 1 and 4.



e_a = phase a line-neutral voltage
i_a = phase a line current

E_a = voltage phasor
I_{a1} = fundamental current phasor

Figure 10.11 Variation of phase displacement between voltage and current of phase a with delay angle

The direct current I_d is constant by assumption (L_d in Figure 10.7 prevents I_d from changing). Since each valve conducts for a period of 120°, the alternating line currents appear as rectangular pulses of magnitude I_d and duration of 120° or $2\pi/3$ rad. With the assumption that there is no overlap, the shape of the alternating line currents is independent of α. Only the phase displacement changes with α.

The fundamental frequency component of the alternating line current can be determined by Fourier analysis of the current wave shape shown in Figure 10.12.

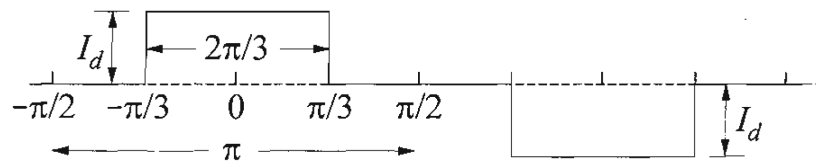


Figure 10.12 Line current waveform

The peak value of the fundamental frequency component of the alternating line current is

$$
\begin{aligned}
I_{LM} &= \frac{2}{\pi}\int_{-\pi/3}^{\pi/3} I_d \cos x\,dx = \frac{2}{\pi} I_d \sin x \Big|_{-60^\circ}^{60^\circ} \\
&= \frac{2}{\pi} I_d [\sin 60^\circ - \sin(-60^\circ)] \\
&= \frac{2}{\pi}\sqrt{3} I_d = 1.11 I_d
\end{aligned}
\tag{10.5A}
$$

The RMS value of the fundamental frequency component of the alternating line current is

$$
\begin{aligned}
I_{L1} &= \frac{I_{LM}}{\sqrt{2}} = \frac{2\sqrt{3}}{\pi\sqrt{2}} I_d \\
&= \frac{\sqrt{6}}{\pi} I_d = 0.78 I_d
\end{aligned}
\tag{10.5B}
$$

With losses in the converter neglected, the ac power must equal the dc power. Therefore,

$$
\begin{aligned}
3 E_{LN} I_{L1} \cos\phi &= V_d I_d \\
&= (V_{do} \cos\alpha) I_d
\end{aligned}
$$

where

E_{LN} = RMS value of the line-to-neutral voltage
ϕ = angle by which fundamental line current lags the line-to-neutral source voltage as shown in Figure 10.11

Substituting for V_{d0} from Equation 10.3B and for I_{L1} from Equation 10.5B, we have

$$\left(3E_{LN}\frac{\sqrt{6}}{\pi}I_d\right)\cos\phi = \left(\frac{3\sqrt{6}}{\pi}E_{LN}I_d\right)\cos\alpha$$

Hence, the power factor of the fundamental wave is

$$\cos\phi = \cos\alpha \tag{10.6}$$

The term $\cos\phi$ is referred to by some authors as the "vector power factor" or "displacement factor" [2].

The converter thus operates as a device that converts alternating to direct current (or direct to alternating current) so that the current ratio is fixed but the voltage ratio varies with the ignition delay caused by grid or gate control.

The ignition delay α shifts the current wave and its fundamental component by an angle $\phi=\alpha$, as shown in Figure 10.11. With $\alpha=0°$, the fundamental current component (i_{a1}) is in phase with the phase voltage e_a; the active power ($P_a=E_aI_{a1}\cos\phi$) is positive and the reactive power ($Q_a=E_aI_{a1}\sin\phi$) is zero. As α increases from 0° to 90°, P_a decreases and Q_a increases. At $\alpha=90°$, P_a is zero and Q_a is maximum. As α increases from 90° to 180°, P_a becomes negative and increases in magnitude; Q_a remains positive and decreases in magnitude. At $\alpha=180°$, P_a is negative maximum and Q_a is zero. We see that the converter, whether it is acting as a rectifier or as an inverter, draws reactive power from the ac system.

Analysis including commutation overlap

Due to the inductance L_c of the ac source (see Figure 10.7), the phase currents cannot change instantly. Therefore, the transfer of current from one phase to another requires a finite time, called the commutation time or overlap time. The corresponding *overlap* or *commutation angle* is denoted by μ.

In normal operation, the overlap angle is less than 60°; typical full-load values are in the range of 15° to 25°. With $0°<\mu<60°$, during commutation three valves conduct simultaneously. However, between commutations only two valves conduct. A new commutation begins every 60° and lasts for an angular period of μ. Therefore, the angular period when two valves conduct with no ignition delay (i.e., $\alpha=0$) is $60°-\mu$, as shown in Figure 10.13. During each commutation period, the current in the incoming valve increases from 0 to I_d, and the current in the outgoing valve reduces from I_d to 0. For simplicity, in Figure 10.13 we have identified only the valve conduction periods, but not the valve currents.

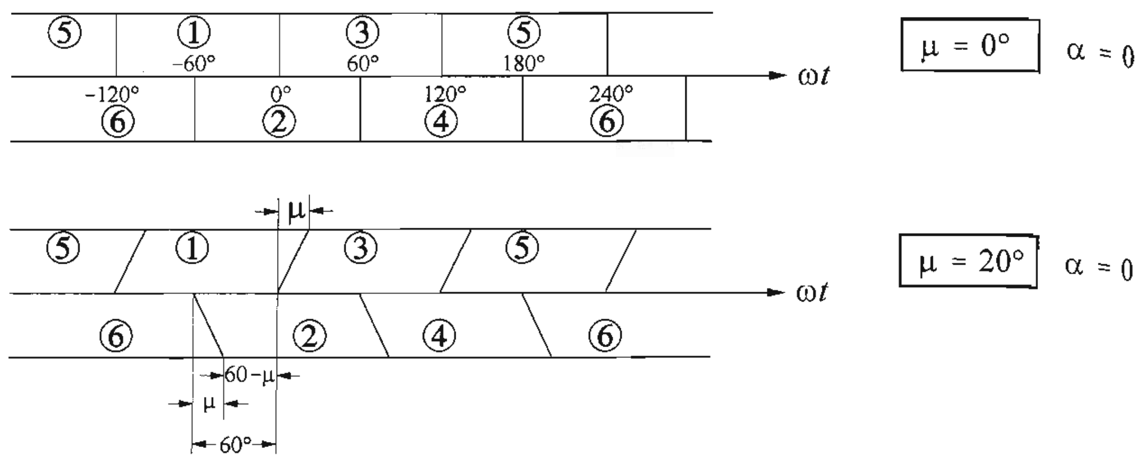


Figure 10.13 Effect of overlap angle on periods of conduction of valves

If $60° \leq \mu < 120°$, an abnormal mode of operation occurs in which alternately three and four valves conduct [2]. Here we will consider only the normal operation when μ is less than 60°.

Let us analyze the effect of overlap by considering the commutation from valve 1 to valve 3. Figure 10.14 shows the periods of valve conduction, when ignition delay is included. The commutation begins when $\omega t=\alpha$ (delay angle) and ends when $\omega t=\alpha+\mu=\delta$, where δ is *extinction angle* (equal to the sum of the delay angle α and commutation angle μ).

At the beginning of commutation ($\omega t=\alpha$): $i_1=I_d$ and $i_3=0$

At the end of commutation ($\omega t=\alpha+\mu=\delta$): $i_1=0$ and $i_3=I_d$

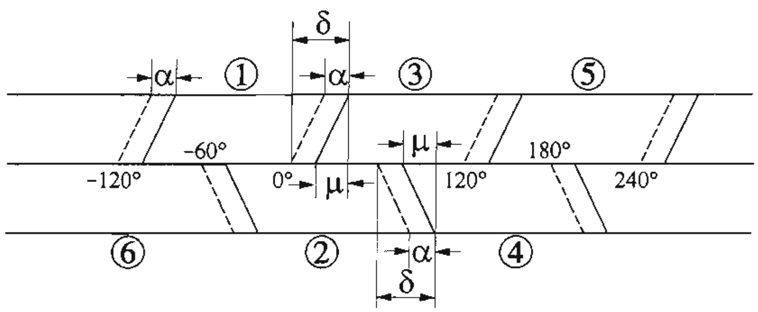
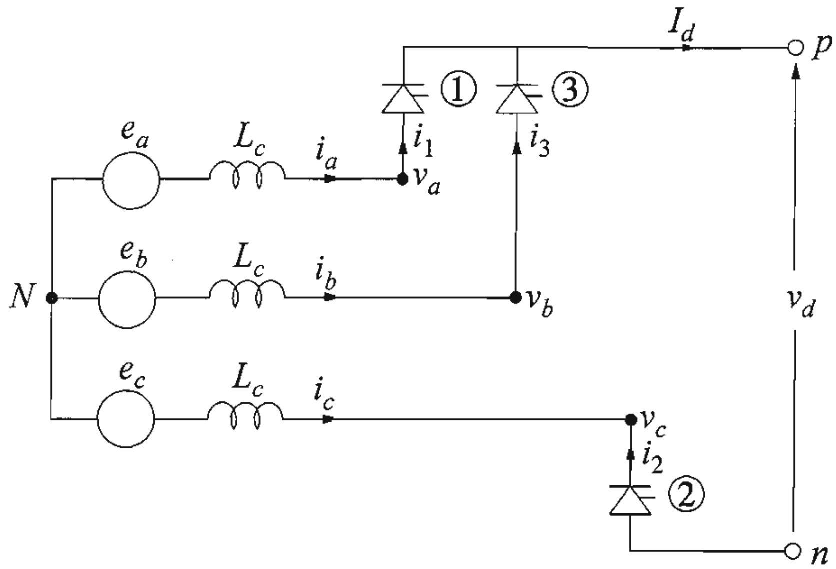


Figure 10.14 Periods of valve conduction with ignition delay

During the period of commutation, valves 1, 2 and 3 are conducting and the effective converter circuit is as shown in Figure 10.15. From the figure, for the loop containing valves 1 and 3, we have

$$e_b - e_a = L_c\frac{di_3}{dt} - L_c\frac{di_1}{dt}$$



Note: Non-conducting valves not shown.

Figure 10.15 Equivalent circuit during commutation

The voltage $e_b - e_a$ is called the "commutating voltage." From Equation 10.2, it is equal to $\sqrt{3}E_m \sin\omega t$. Therefore,

$$\sqrt{3}E_m \sin\omega t = L_c \frac{di_3}{dt} - L_c \frac{di_1}{dt}$$

Since $i_1 = I_d - i_3$,

$$\frac{di_1}{dt} = 0 - \frac{di_3}{dt}$$

Hence,

$$e_b - e_a = \sqrt{3}E_m \sin\omega t = 2L_c \frac{di_3}{dt} \tag{10.7A}$$

or

$$\frac{di_3}{dt} = \frac{\sqrt{3}E_m}{2L_c} \sin\omega t \tag{10.7B}$$

Taking a definite integral with respect to t, with the lower limit corresponding to the beginning of commutation ($\omega t = \alpha$ or $t = \alpha/\omega$) and a running upper limit, we have

$$\int_0^{i_3} di_3 = \frac{\sqrt{3}E_m}{2L_c}\int_{\alpha/\omega}^{t}\sin\omega t\,dt$$

Integration of the above equation yields

$$i_3 = \frac{\sqrt{3}E_m}{2\omega L_c}(\cos\alpha - \cos\omega t) \tag{10.8A}$$

$$= I_{S2}(\cos\alpha - \cos\omega t)$$

where

$$I_{S2} = \frac{\sqrt{3}E_m}{2\omega L_c} \tag{10.8B}$$

The current i_3 of the incoming valve during commutation consists of a constant term ($I_{S2}\cos\alpha$) and a sinusoidal term ($-I_{S2}\cos\omega t$) lagging the commutating voltage by 90°. This is to be expected because what we have here is a line-to-line short-circuit through an inductance of $2L_c$. The constant component of i_3 depends on α; it serves to make i_3=0 at the beginning of commutation.

As shown in Figure 10.16, the current during commutation is a segment of a sinusoidal current with a peak value of $I_{S2}=\sqrt{3}E_m/(2\omega L_c)$. The shape of the segment is a function of the control angle α. Therefore, the overlap angle depends on I_d, L_c and α.

During commutation, the shape of i_1 satisfies $i_1=I_d-i_3$. For α nearly equal to 0° (or 180°), the commutation period or the overlap is the greatest. The overlap is the shortest when α=90°, since i_3 is associated with the segment of the sine wave which is nearly linear. Also, if the source voltage E_m is lowered or if I_d is increased, the overlap increases.

Voltage reduction due to commutation overlap:

During commutation,

$$v_a = v_b = e_b - L_c\frac{di_3}{dt}$$

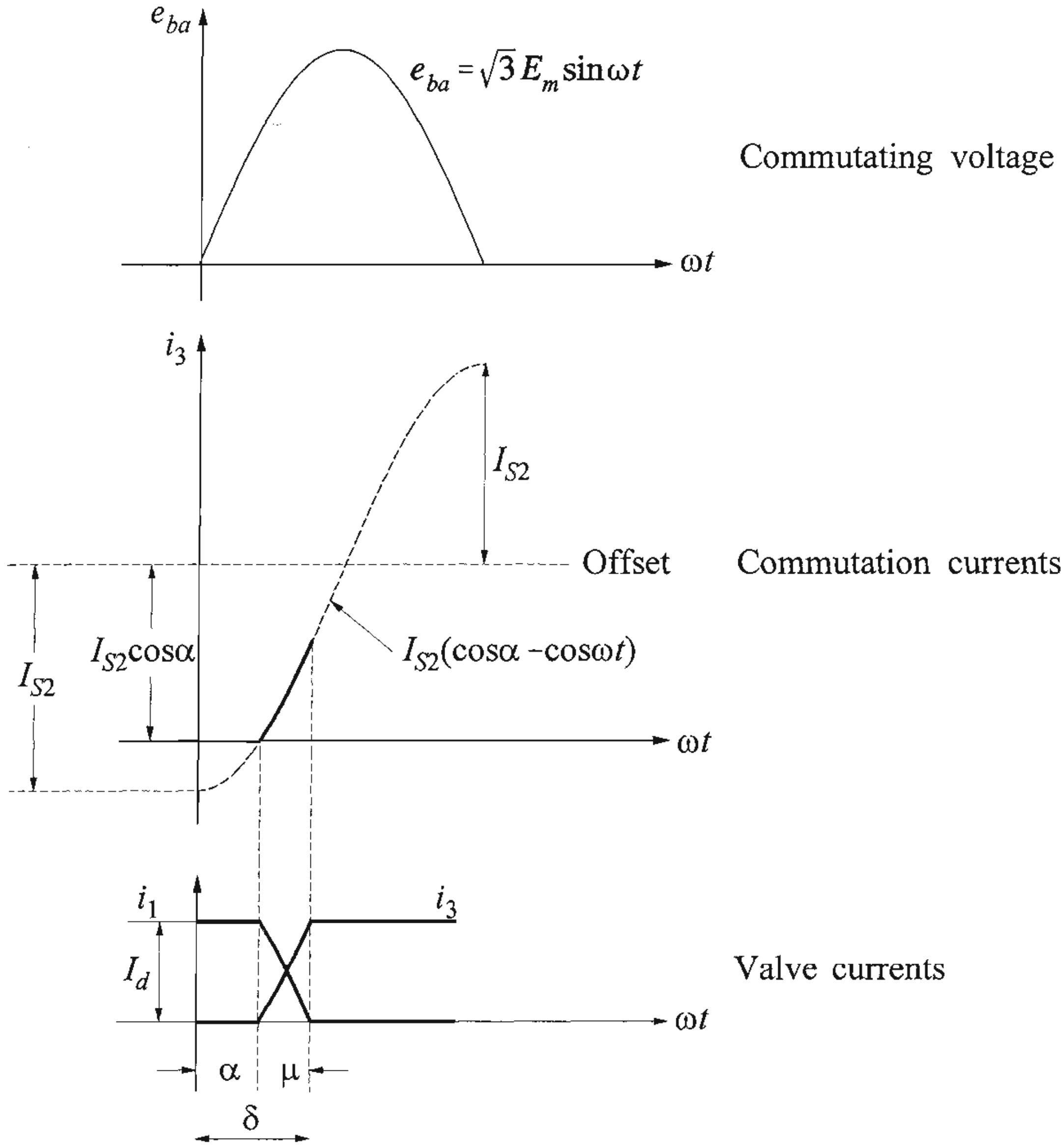


Figure 10.16 Valve currents during commutation in relation to commutating voltage

From Equation 10.7A,

$$L_c \frac{di_3}{dt} = \frac{e_b - e_a}{2}$$

Hence,

$$v_a = v_b = e_b - \frac{e_b - e_a}{2}$$

$$= \frac{e_a + e_b}{2}$$

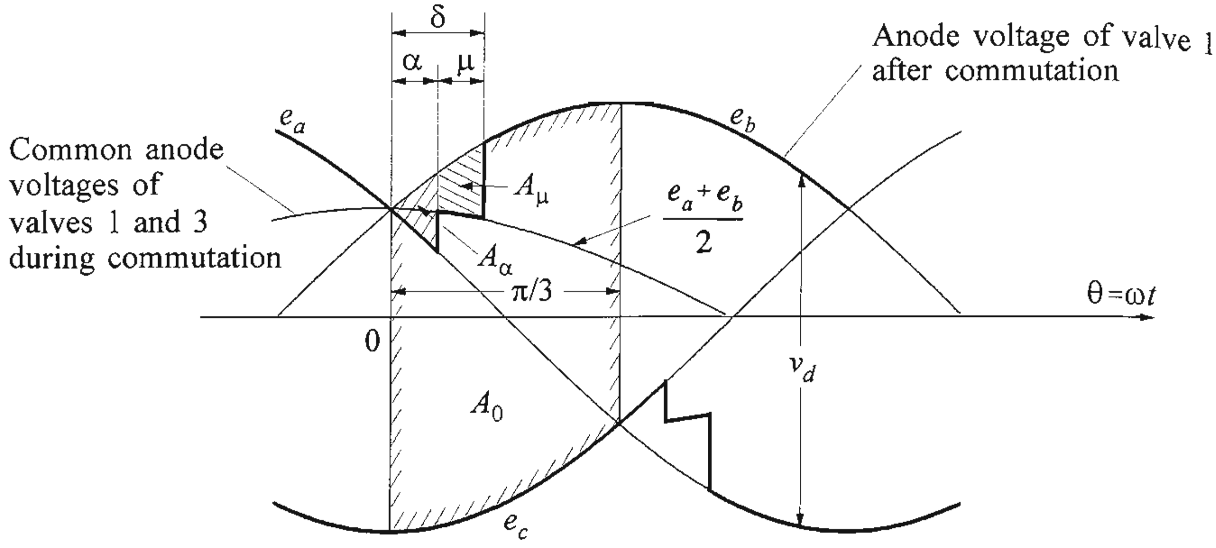


Figure 10.17 Voltage waveforms showing the effect of overlap during commutation from valve 1 to valve 3

Because of the overlap, the voltage of the terminal p (see Figure 10.15) immediately after $\omega t = \alpha$ recovers to $(e_a + e_b)/2$, instead of e_b. Therefore, as shown in Figure 10.17, the effect of the overlap is measured by subtracting an area A_μ from the area A_0, once every 60° (π/3 rad).

$$A_\mu = \int_\alpha^\delta \left(e_b - \frac{e_a + e_b}{2} \right) d\theta = \int_\alpha^\delta \frac{e_b - e_a}{2} d\theta$$

$$= \frac{\sqrt{3}E_m}{2} \int_\alpha^\delta \sin\theta \, d\theta = \frac{\sqrt{3}E_m}{2}(\cos\alpha - \cos\delta)$$

The corresponding average voltage drop (due to overlap) is given by

$$\Delta V_d = \frac{A_\mu}{\pi/3} = \frac{3}{\pi}\frac{\sqrt{3}}{2}E_m(\cos\alpha - \cos\delta)$$
$$= \frac{V_{d0}}{2}(\cos\alpha - \cos\delta) \qquad (10.9)$$

where V_{d0} is the ideal no-load voltage given by Equation 10.3.

From Equation 10.8A, the current i_3 during commutation is

$$i_3 = \frac{\sqrt{3}E_m}{2\omega L_c}(\cos\alpha - \cos\omega t)$$

Since at the end of the commutation $\omega t = \delta$ and $i_3 = I_d$,

$$I_d = \frac{\sqrt{3}E_m}{2\omega L_c}(\cos\alpha - \cos\delta) \tag{10.10}$$

$$= I_{S2}(\cos\alpha - \cos\delta)$$

Hence,

$$\frac{\sqrt{3}E_m}{2}(\cos\alpha - \cos\delta) = I_d \omega L_c$$

Substituting in Equation 10.9 gives

$$\Delta V_d = \frac{3}{\pi} I_d \omega L_c$$

With commutation overlap and ignition delay, the reduction in direct voltage is represented by areas A_α and A_μ; the direct voltage is given by

$$V_d = V_{d0}\cos\alpha - \Delta V_d \tag{10.11}$$

$$= V_{d0}\cos\alpha - R_c I_d$$

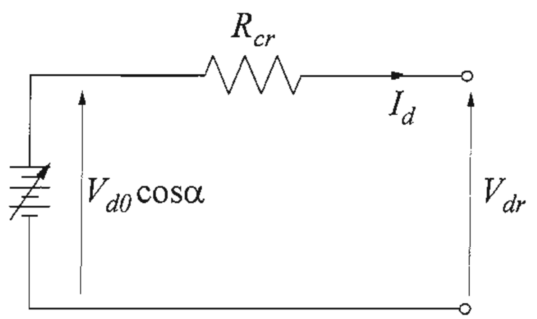
where

$$R_c = \frac{3}{\pi}\omega L_c = \frac{3}{\pi} X_c \tag{10.12}$$

and R_c is called the "equivalent commutating resistance." It accounts for the voltage drop due to commutation overlap. It does not, however, represent a real resistance and consumes no power.

Rectifier operation

The equivalent circuit of the bridge rectifier based on the above analysis is given in Figure 10.18. The direct voltage and current in the equivalent circuit are the average values. The internal voltage is a function of the ignition angle α. The overlap angle μ does not explicitly appear in the equivalent circuit; the effect of commutation overlap is represented by R_{cr}. The voltage wave shapes and periods of valve conduction for rectifier mode of operation, including commutation overlap, are shown in Figure 10.19(a).



$$R_{cr} = \frac{3}{\pi} X_{cr}$$

$$V_{d0} = \frac{3\sqrt{3}}{\pi} E_m$$

Figure 10.18 Bridge rectifier equivalent circuit

Inverter operation

If there is no commutation overlap, $V_d = V_{d0}\cos\alpha$. Therefore, V_d reverses when $\alpha = 90°$.

With overlap,

$$V_d = V_{d0}\cos\alpha - \Delta V_d$$

Substituting for ΔV_d from Equation 10.9, we have

$$\begin{aligned} V_d &= V_{d0}\cos\alpha - \frac{V_{d0}}{2}(\cos\alpha - \cos\delta) \\ &= \frac{V_{d0}}{2}(\cos\alpha + \cos\delta) \end{aligned} \tag{10.13}$$

The transitional value of the ignition delay angle, α_t, beyond which inversion takes place is given by

$$\cos\alpha_t + \cos\delta_t = 0$$

or

$$\begin{aligned} \alpha_t &= \pi - \delta_t = \pi - \alpha_t - \mu \\ &= \frac{\pi - \mu}{2} \end{aligned} \tag{10.14}$$

The effect of the overlap is thus to reduce α_t from 90° to $90° - \mu/2$.

At first sight, it may seem strange to delay the firing pulse until the actual anode voltage becomes negative. We should, however, realize that commutation is always possible as long as the commutating voltage ($e_{ba} = e_b - e_a$) is positive and as long as the outgoing valve will have reversed voltage applied to it after it extinguishes.

Since valves conduct in only one direction, the current in a converter cannot be reversed. A reversal of V_d results in a reversal of power. An alternating voltage must exist on the primary side of the transformer for inverter operation. The direct voltage of the inverter opposes the current, as in a dc motor, and is called a countervoltage or back voltage. The applied direct voltage from the rectifier forces current through the inverter valves against this back voltage.

Figure 10.19(b) shows the voltage wave shapes and periods of valve conduction for inverter mode of operation. For successful commutation, the changeover from the outgoing valve to the incoming valve must be complete before the commutating voltage becomes negative. For example, commutation from valve 1 to valve 3 is possible only when e_b is more positive than e_a; the current changeover from valve 1 to valve 3 must be complete before e_a becomes more positive than e_b with sufficient margin to allow for valve de-ionization.

For description of rectifier operation, we use the following angles:

α = ignition delay angle
μ = overlap angle
δ = extinction delay angle = $\alpha + \mu$

As illustrated in Figure 10.20, α is the angle by which ignition is delayed from the instant at which the commutating voltage (e_{ba} for valve 3) is zero and increasing.

The inverter operation may also be described in terms of α and δ defined in the same way as for the rectifier, but having values between 90° and 180°. However, the common practice is to use *ignition advance angle* β and *extinction advance angle* γ for describing inverter performance. These angles are defined by their advance with respect to the instant (ωt=180° for ignition of valve 3 and extinction of valve 1) when the commutating voltage is zero and decreasing, as shown in Figure 10.20. From the figure, we see that

$\beta = \pi - \alpha$ = ignition advance angle
$\gamma = \pi - \delta$ = extinction advance angle
$\mu = \delta - \alpha = \beta - \gamma$ = overlap

Since $\cos\alpha = -\cos\beta$ and $\cos\delta = -\cos\gamma$, Equations 10.10 and 10.13 may be written in terms of γ and β as follows:

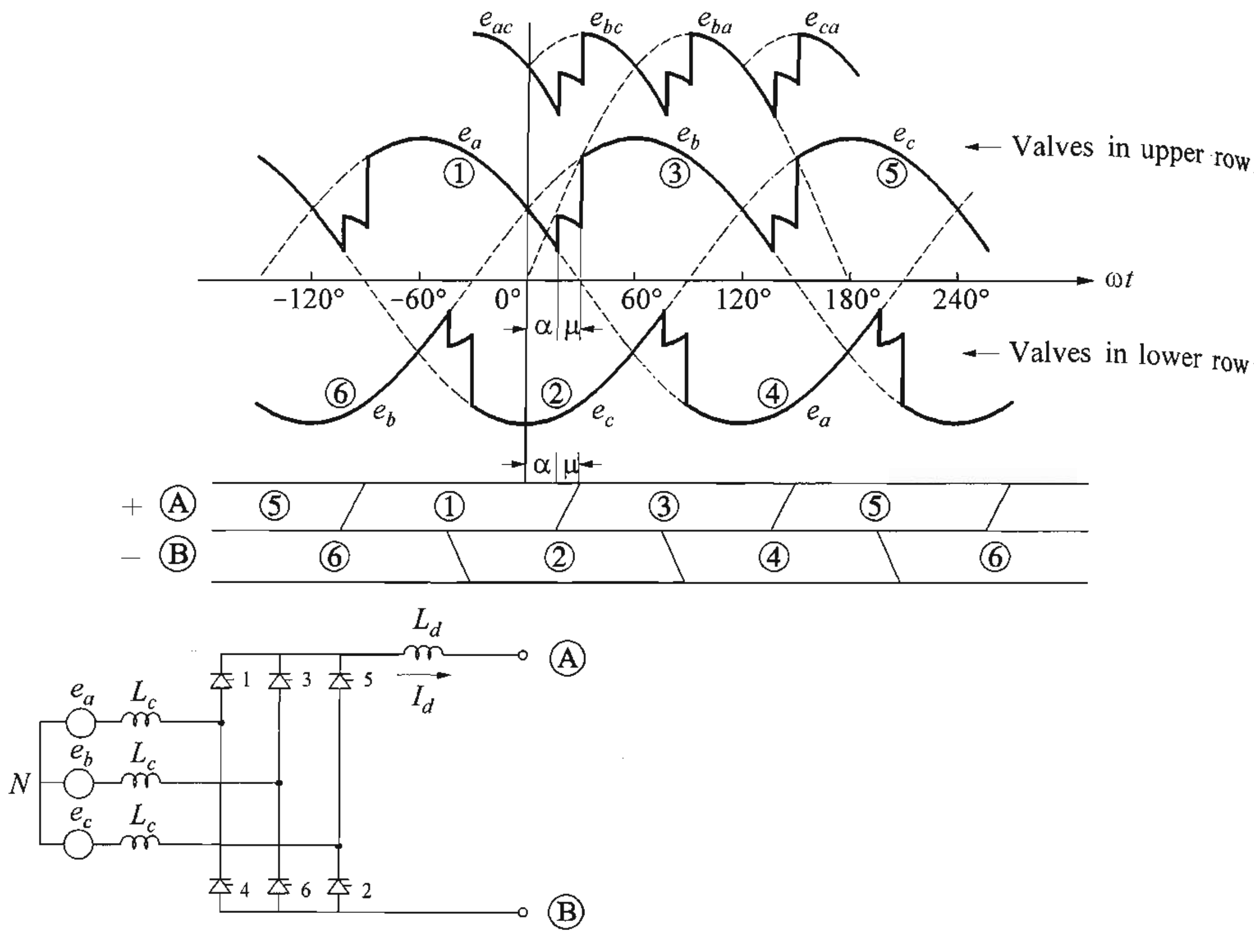
$$I_d = I_{S2}(\cos\gamma - \cos\beta) \tag{10.15}$$

$$V_d = V_{d0}\frac{\cos\gamma + \cos\beta}{2} \tag{10.16}$$

or

$$V_d = V_{d0}\cos\beta + R_c I_d \tag{10.17A}$$

(a) Rectifier mode:



(b) Inverter mode:
α > 120°

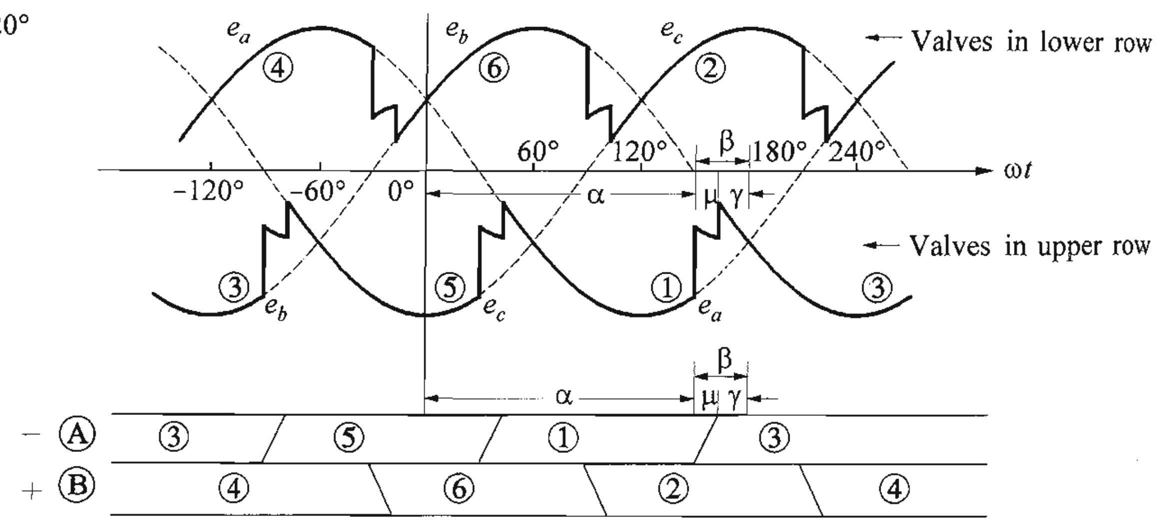
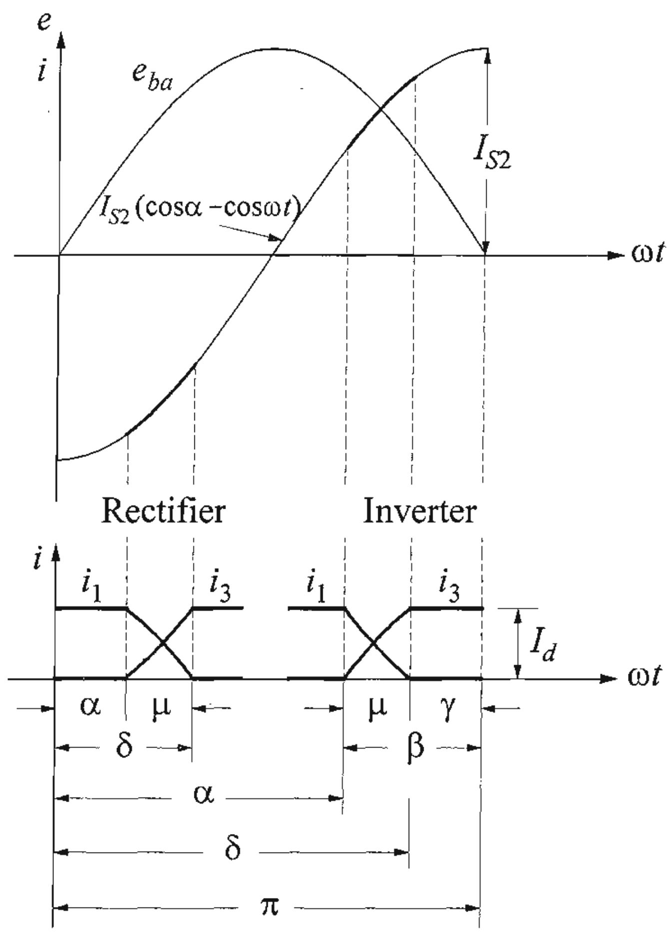


Figure 10.19 Voltage wave shapes and valve conduction periods

Converter Angle Definitions



e_{ba} = commutating voltage

$I_{S2}(\cos\alpha - \cos\omega t)$ = current during commutating period

i_1 = current in valve 1

i_3 = current in valve 3

Figure 10.20 Angles used in the description of rectifier and inverter operations

or

$$V_d = V_{d0}\cos\gamma - R_c I_d \tag{10.17B}$$

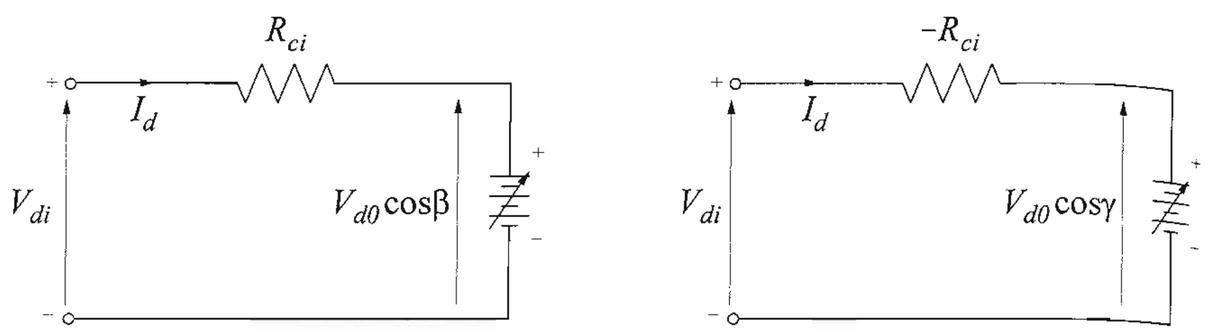
The inverter voltage, considered negative in general converter equations, is usually taken as positive when written specifically for an inverter.

Based on the above equations, the inverter may be represented by the two alternative equivalent circuits shown in Figure 10.21.

Relationship between ac and dc quantities

From Equation 10.13, the average direct voltage V_d is given by

$$V_d = V_{d0}\cos\alpha - \Delta V_d = V_{d0}\frac{\cos\alpha + \cos\delta}{2} \tag{10.18A}$$



(a) In terms of β (b) In terms of γ

Figure 10.21 Inverter equivalent circuits (with V_{di} positive)

Substituting for V_{d0} from Equation 10.3B in terms of RMS line-to-neutral voltage E_{LN}, we get

$$V_d = \frac{3\sqrt{6}}{\pi}\frac{\cos\alpha + \cos\delta}{2}E_{LN} \tag{10.18B}$$

With losses neglected, ac power is equal to the dc power:

$$P_{ac} = P_{dc}$$

Hence,

$$3E_{LN}I_{L1}\cos\phi = V_d I_d$$

where

E_{LN} = RMS line-to-neutral voltage
I_{L1} = RMS fundamental frequency current

From Equation 10.18,

$$3E_{LN}I_{L1}\cos\phi = \frac{3\sqrt{6}}{\pi}\frac{\cos\alpha + \cos\delta}{2}E_{LN}I_d$$

Hence,

$$I_{L1}\cos\phi = \left(\frac{\sqrt{6}}{\pi}I_d\right)\left(\frac{\cos\alpha + \cos\delta}{2}\right) \tag{10.19}$$

From Equation 10.5B, with $\mu=0$

$$I_{L1} = \frac{\sqrt{6}}{\pi} I_d$$

Denoting this value of I_{L1} (when $\mu=0$) by I_{L10}, Equation 10.19 can be written as

$$I_{L1}\cos\phi = I_{L10}\left(\frac{\cos\alpha + \cos\delta}{2}\right) \tag{10.20}$$

where

$$I_{L10} = \frac{\sqrt{6}}{\pi} I_d \tag{10.21}$$

Approximate expressions

As an approximation I_{L1} may be considered equal to I_{L10}:

$$I_{L1} \approx I_{L10} = \frac{\sqrt{6}}{\pi} I_d \tag{10.22}$$

The above relationship is exact if $\mu=0°$; with $\mu=60°$ the error is 4.3%, and with $\mu<30°$ (normal value) the error is less than 1.1% [2].

It follows that the power factor is given by

$$\cos\phi \approx \frac{\cos\alpha + \cos\delta}{2} \tag{10.23}$$

As a result of the approximation, from Equation 10.18A,

$$V_d \approx V_{d0}\cos\phi \tag{10.24A}$$

Hence,

$$\cos\phi \approx \frac{V_d}{V_{d0}} \tag{10.24B}$$

From Equation 10.11, $V_d = V_{d0}\cos\alpha - R_c I_d$. Hence,

$$\cos\phi \approx \cos\alpha - \frac{R_c I_d}{V_{d0}} \tag{10.25}$$

Substituting for V_{d0} from Equation 10.3A in Equation 10.24A, we get

$$V_d \approx \frac{3\sqrt{6}}{\pi} E_{LN} \cos\phi \tag{10.26}$$

We see from Equation 10.22 that the converter has essentially fixed current ratio I_d/I_{L1}, the variation with load being only a few percent. The power factor $\cos\phi$, as seen from Equation 10.25, depends on load in addition to ignition delay angle α.

10.2.3 Converter Transformer Rating

The RMS value of the transformer secondary current (total and not just the fundamental frequency component) I_{TRMS} is given by

$$I_{TRMS}^2 = \frac{1}{T}\int_0^T i^2(t)\,dt$$

The alternating line-current wave consists of rectangular pulses of amplitude I_d and width $2\pi/3$ rad as shown in Figure 10.12. Therefore,

$$\begin{aligned} I_{TRMS}^2 &= \frac{1}{\pi}\int_{-\pi/2}^{\pi/2} i^2(t)\,dt \\ &= \frac{1}{\pi}\int_{-\pi/3}^{\pi/3} I_d^2\,dt \\ &= \frac{2}{3} I_d^2 \end{aligned}$$

and hence,

$$I_{TRMS} = \sqrt{2/3}\, I_d \tag{10.27}$$

The RMS value of the line-to-neutral transformer secondary voltage is given by

$$E_{LN} = \frac{\pi}{3\sqrt{6}} V_{d0}$$

Transformer volt-ampere rating is given by

$$
\begin{aligned}
\text{3-phase rating} &= 3E_{LN}I_{TRMS} \\
&= 3\left(\frac{\pi}{3\sqrt{6}}\right)V_{d0}\sqrt{\frac{2}{3}}I_d \\
&= \frac{\pi}{3}V_{d0}I_d \\
&= 1.0472\,(\text{ideal no-load direct voltage})\,(\text{rated direct current})
\end{aligned}
\tag{10.28}
$$

10.2.4 Multiple-Bridge Converters

Two or more bridges are connected in series to obtain as high a direct voltage as required. The bridges are in series on the dc side and parallel on the ac side. A bank of transformers is connected between the ac source and bridge-connected valves. The ratios of the transformers are adjustable under load.

In practice, multiple-bridge converters have an even number of bridges arranged in pairs so as to result in a 12-pulse arrangement. As shown in Figure 10.22,

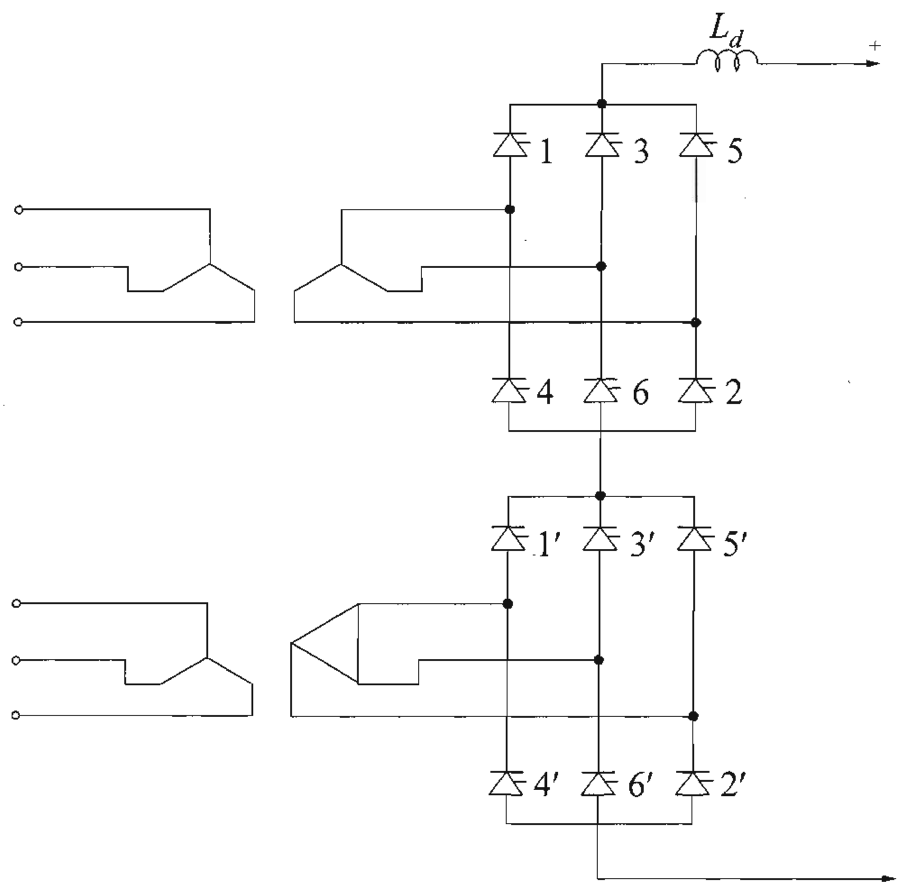


Figure 10.22 12-pulse bridge converter

two banks of transformers, one connected Y-Y and the other Y-Δ, are used to supply each pair of bridges. The three-phase voltages supplied at one bridge are displaced by 30° from those supplied at the other bridge. The ac wave shapes for the two bridges, as illustrated in Figure 10.23, add up so as to produce a wave shape which is more sinusoidal than the current waves for each of the 6-pulse bridges. As we will see in Section 10.6, with a 12-pulse arrangement, *fifth and seventh harmonics are effectively eliminated* on the ac side. This reduces the cost of harmonic filters significantly.

In addition, with a 12-pulse bridge arrangement, the dc voltage ripple is reduced; sixth and eighteenth harmonics are eliminated (6-pulse bridges have multiples of sixth harmonics on the dc side whereas 12-pulse bridges have only multiples of the twelfth harmonic).

For converters having more than two bridges, higher pulse numbers are possible: 18-pulse, three-bridge converter; 24-pulse, four-bridge converters. The transformer connections required are more complex than those for 12-pulse converters. Therefore, it is more practical to use 12-pulse converters and provide the necessary filtering.

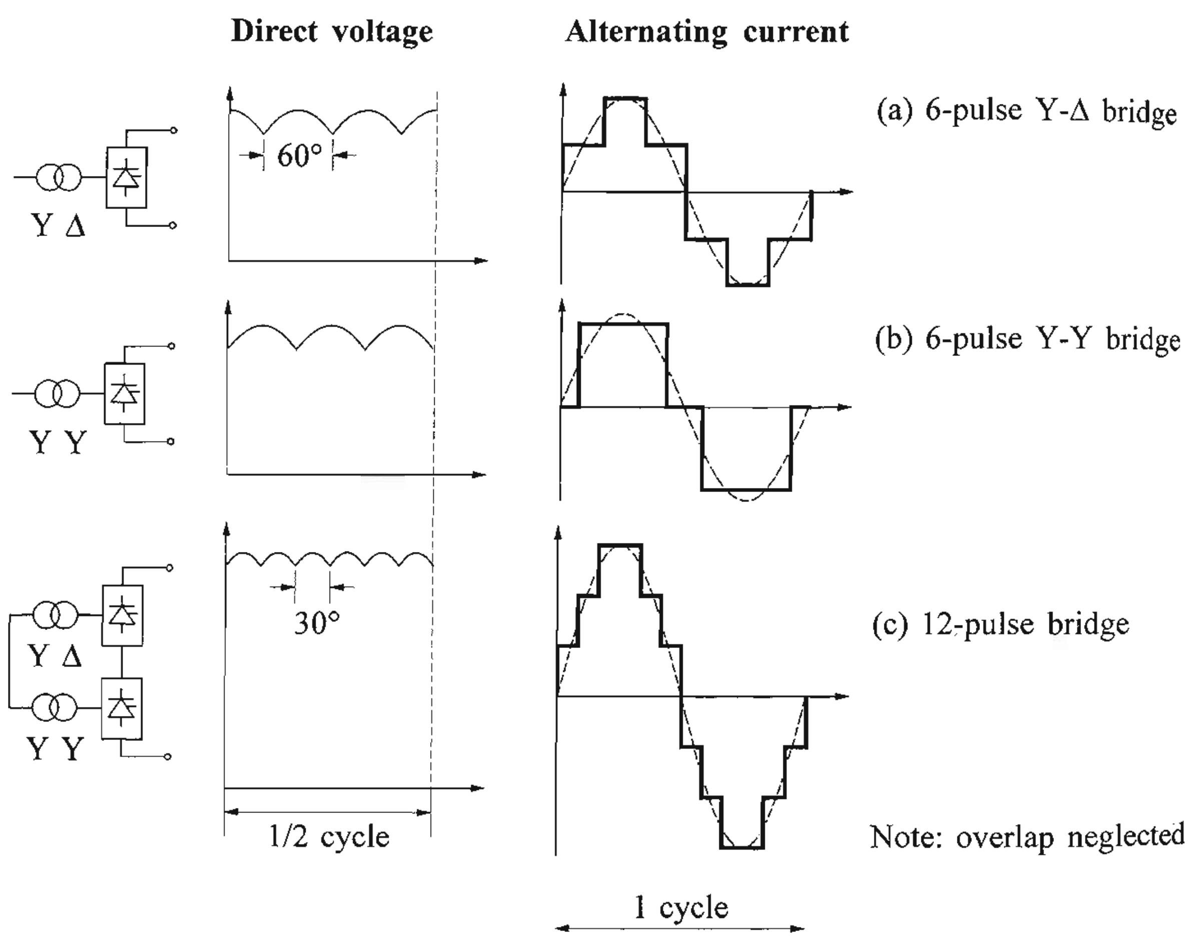
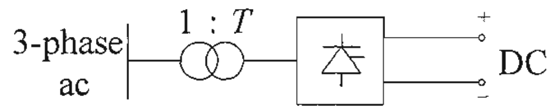


Figure 10.23 Direct voltage and alternating current wave shapes

Relationships between ac and dc quantities, with multiple bridges

Let

B = no. of bridges in series
T = transformer ratio



The ideal no-load voltage (corresponding to Equation 10.3C) is

$$V_{d0} = \frac{3\sqrt{2}}{\pi} BTE_{LL} = 1.3505BTE_{LL} \qquad (10.29)$$

Since voltage drop per bridge is $I_d(3X_c/\pi)$ and there are B bridges in series, the dc voltage (corresponding to Equations 10.11) is given by

$$V_d = V_{d0}\cos\alpha - I_d B\left(\frac{3}{\pi}X_c\right) \qquad (10.30A)$$

or

$$V_d = V_{d0}\cos\gamma - I_d B\left(\frac{3}{\pi}X_c\right) \qquad (10.30B)$$

The dc voltage in terms of the power factor per Equation 10.24A is given by

$$V_d \approx V_{d0}\cos\phi \qquad (10.31)$$

However, with multiple bridges, V_{d0} is given by Equation 10.29. The average dc output voltage of a 12-pulse bridge is, therefore, twice that of a 6-pulse bridge converter. The RMS value of the fundamental frequency component of the total alternating current (corresponding to Equation 10.22) is given by

$$I_{L1} \approx \frac{\sqrt{6}}{\pi} BTI_d = 0.78BTI_d \qquad (10.32)$$

Example 10.1

A three-phase, 12-pulse rectifier is fed from a transformer with nominal voltage ratings of 220 kV/110 kV.

(a) If the primary voltage is 230 kV and the effective turns ratio T is 0.48, determine the dc output voltage when the ignition delay angle α is 20° and the commutation angle μ is 18°.

(b) If the direct current delivered by the rectifier is 2,000 A, calculate the effective commutating reactance X_c, RMS fundamental component of alternating current, power factor cosϕ, and reactive power at the primary side of the transformer.

Solution

(a) A 12-pulse bridge circuit comprises two 6-pulse bridges. Hence B=2.

The no-load direct voltage is

$$V_{d0} = \frac{3\sqrt{2}}{\pi} BTE_{LL}$$

$$= 1.3505 \times 2 \times 0.48 \times 230$$

$$= 298.18 \quad \text{kV}$$

The extinction angle is

$$\delta = \alpha + \mu = 20° + 18° = 38°$$

Hence, the reduction in average direct voltage due to commutation overlap is

$$\Delta V_d = V_{d0} \frac{\cos\alpha - \cos\delta}{2}$$

$$= 298.18 \times \frac{\cos 20° - \cos 38°}{2}$$

$$= 22.61 \quad \text{kV}$$

The dc output voltage is

$$V_d = V_{d0} \cos\alpha - \Delta V_d$$

$$= 298.18 \cos 20° - 22.61$$

$$= 257.58 \quad \text{kV}$$

Alternatively,

$$V_d = V_{d0} \frac{\cos\alpha + \cos\delta}{2}$$

$$= 298.18 \times \frac{\cos 20° + \cos 38°}{2}$$

$$= 257.58 \quad \text{kV}$$

(b) $\Delta V_d = BR_cI_d$. Hence,

$$R_c = \frac{\Delta V_d}{BI_d} = \frac{22.61}{2\times 2} = 5.65 \quad \Omega$$

$$X_c = \frac{\pi R_c}{3} = \frac{\pi\times 5.65}{3} = 5.92 \quad \Omega/\text{phase}$$

Fundamental component of alternating current on the primary side is

$$I_{L1} = \frac{\sqrt{6}}{\pi}BTI_d$$

$$= 0.7797\times 2\times 0.48\times 2$$

$$= 1.497 \quad \text{kA}$$

Power factor at the HT bus is

$$\cos\phi \approx \frac{V_d}{V_{d0}} = \frac{257.58}{298.18} = 0.8638$$

Hence, $\phi = \cos^{-1}(0.8638) = 30.25°$

$$P_{ac} = P_{dc} = V_dI_d = 257.58\times 2 = 515.16 \quad \text{MW}$$

$$Q_{HT} = P_{ac}\tan\phi = 515.16\times\tan 30.25° = 300.43 \quad \text{MVAr}$$

The solution is shown in Figure E10.1.

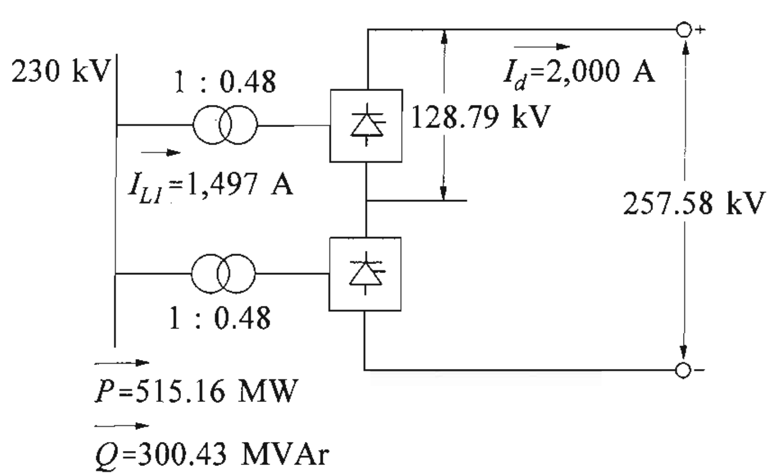


Figure E10.1 ■

10.3 ABNORMAL OPERATION

10.3.1 Arc-back (Backfire)

Arc-back refers to conduction in the reverse direction and is one of the serious problems associated with mercury-arc valves. Since arc-back is reverse conduction, it can occur only when there is inverse voltage across a valve. In rectification each valve is exposed to inverse voltage during approximately two-thirds of each cycle. Therefore, arc-backs are more common during rectification than during inversion.

Arc-back is a random phenomenon. Among the factors that tend to increase its occurrence are high-peak inverse voltage, overcurrent, high rate of change of current at the end of conduction, condensation of mercury vapour on anodes, and high rate of increase of inverse voltage. The effect of the arc-back is to place a short-circuit across two phases of the secondary of the converter transformers. These short-circuit currents subject the transformers and valves to much greater current than in normal operation. The transformer windings must be firmly braced to withstand more numerous short-circuits than ordinary power transformers; this adds to the cost. The valves require increased maintenance.

To remove an arc-back, current is diverted into a bypass valve. The bypass valve is a separate valve connected across a 6-pulse valve group. This valve has a higher current rating than other valves and is capable of carrying 1 pu direct current for about 60 seconds. The control grid of the bypass valve is normally blocked. When a bridge is to be bypassed, its bypass valve is unblocked and the main valves are simultaneously blocked by discontinuing the transmission of positive pulses to their grids. The direct current shifts from the main valves to the bypass valve in a few milliseconds. By simultaneously unblocking the main valve and blocking the bypass valve, the direct current can be transferred back to the main valves.

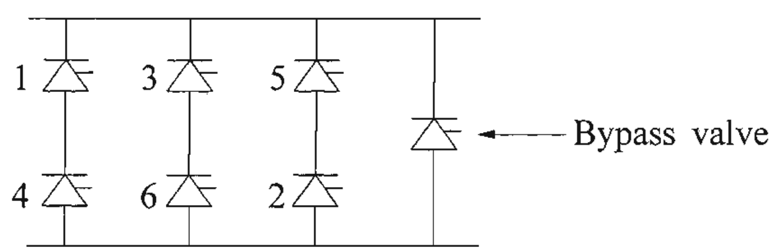


Figure 10.24

Arc-back does not occur in thyristor valves. Thyristors can individually fail in a shorted condition. However, thyristors arrayed into converter valves utilize redundancy and protection to prevent reverse conduction.

10.3.2 Commutation Failure

Failure to complete commutation before the commutating voltage reverses (with sufficient margin for de-ionization) is referred to as commutation failure. It is not due to any misoperation of the valve but to conditions in the circuits outside the valve. Commutation failures are more common with inverters and occur during disturbances such as high direct current or low alternating voltage. A rectifier can have a commutation failure only if the firing circuit fails.

Figure 10.25 illustrates how commutation failure occurs in an inverter. A failure of commutation from valve 1 to valve 3 is considered.

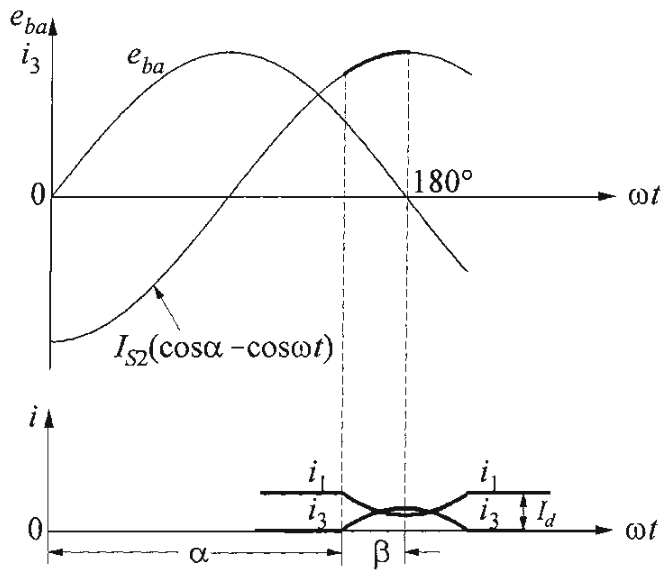


Figure 10.25 Commutation failure in inverters

Because of increased direct current, low alternating voltage (possibly caused by an ac system short-circuit), late ignition, or a combination of these, valve 1 is not extinguished before e_{ba} reverses. Current in valve 3 will decrease to zero and the valve will extinguish. Valve 1 current will return to I_d, and thus valve 1 will continue to conduct.

As shown in Figure 10.26, when valve 4 fires next, because valve 1 is still conducting, a short is placed across the dc side of the bridge. The zero dc voltage keeps the voltage across valve 5 negative so that valve 5 cannot conduct. Valve 4 is extinguished and valve 6 is ignited in the normal fashion.

Valve 1 thus conducts for one full cycle (3 times normal duration) and extinguishes when valve 3 ignites during the next cycle.

For the period when valves 1 and 4 are both conducting (i.e., for 120°), the inverter dc voltage is zero and hence there is no power flow on the dc system.

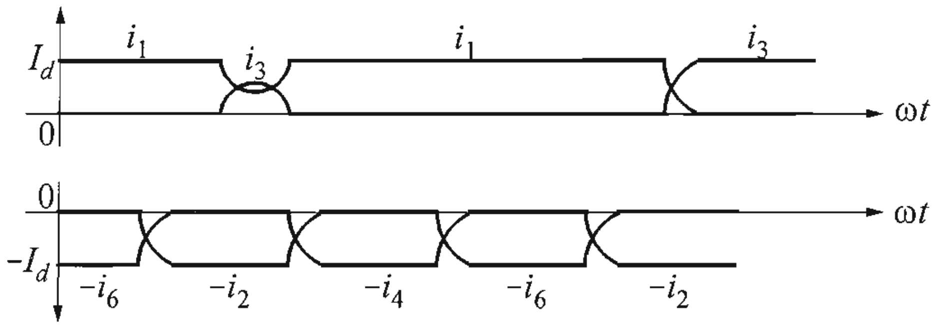


Figure 10.26 Valve currents during commutation failure

Double commutation failure is the failure of two successive commutations in the same cycle. If the unsuccessful commutation from valve 1 to valve 3 were followed by a failure in the commutation from valve 2 to valve 4, valves 1 and 2 would be left conducting until the next cycle when they would be normally conducting again. During the time that only valves 1 and 2 are conducting, the alternating voltages of terminals *a* and *c* appear across the dc terminals.

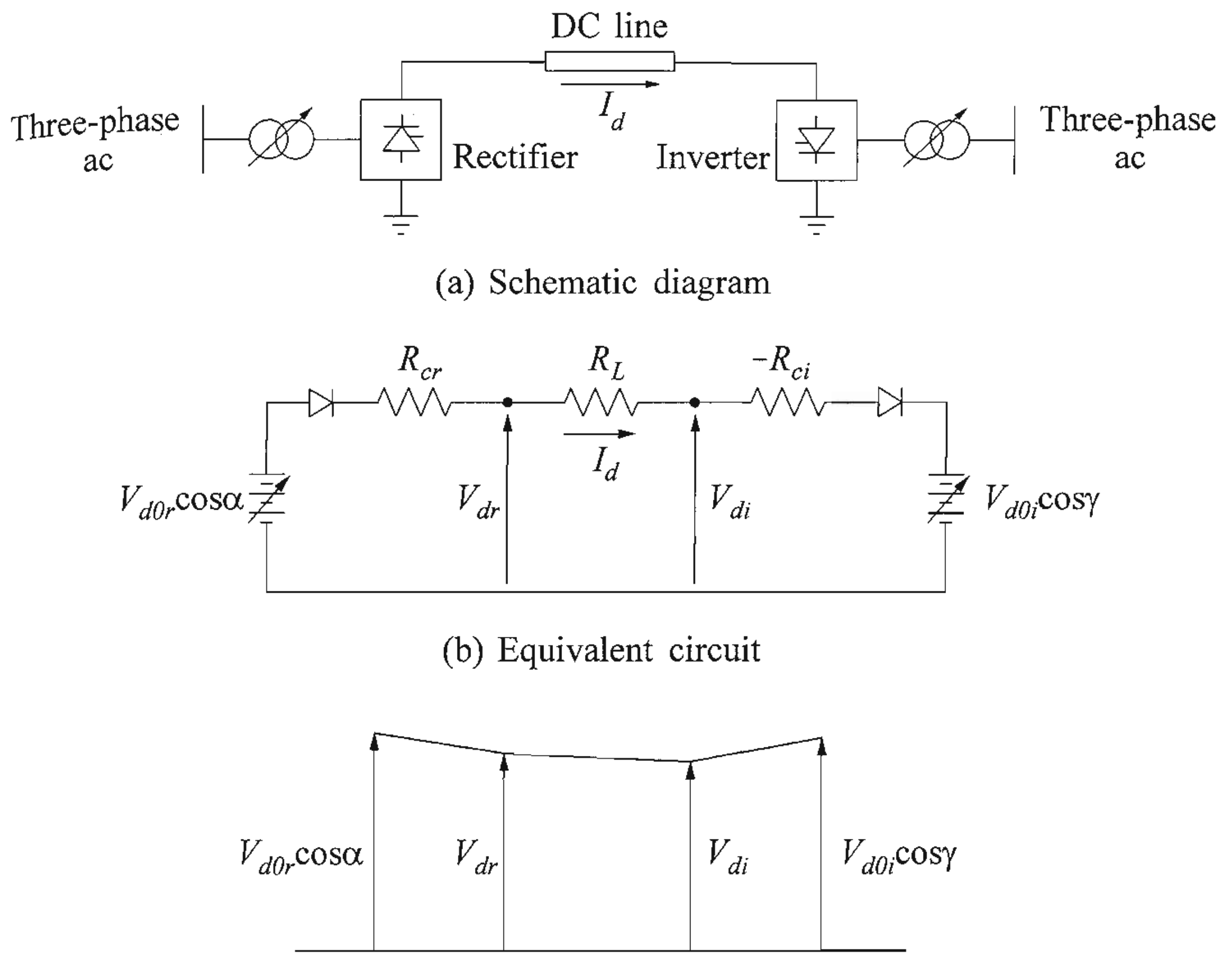
Double commutation failures are very rare. Usually, after one commutation failure, either the firing angle initiating the next commutation is advanced sufficiently by the inverter control, or "double overlap" during the period when valves 1 and 3 as well as valves 2 and 4 are conducting hastens the commutation. Double commutation failure, like the single failure, is self-curing.

10.4 CONTROL OF HVDC SYSTEMS

An HVDC transmission system is highly controllable. Its effective use depends on appropriate utilization of this controllability to ensure desired performance of the power system. With the objectives of providing efficient and stable operation and maximizing flexibility of power control without compromising the safety of equipment, various levels of control are used in a hierarchical manner. In this section, we will describe the principles of operation of these controls, their implementation and their performance during normal and abnormal system conditions.

10.4.1 Basic Principles of Control

Consider the HVDC link shown in Figure 10.27(a). It represents a monopolar link or one pole of a bipolar link. The corresponding equivalent circuit and voltage profile are shown in Figures 10.27(b) and (c), respectively.



(a) Schematic diagram

(b) Equivalent circuit

(c) Voltage profile

Figure 10.27 HVDC transmission link

The direct current flowing from the rectifier to the inverter is

$$I_d = \frac{V_{dor}\cos\alpha - V_{doi}\cos\gamma}{R_{cr}+R_L-R_{ci}} \tag{10.33}$$

The power at the rectifier terminals is

$$P_{dr} = V_{dr}I_d \tag{10.34}$$

and at the inverter terminal is

$$P_{di} = V_{di}I_d = P_{dr}-R_LI_d^2 \tag{10.35}$$

Basic means of control

The direct voltage at any point on the line and the current (or power) can be controlled by controlling the internal voltages ($V_{dor}\cos\alpha$) and ($V_{doi}\cos\gamma$). This is accomplished by grid/gate control of the valve ignition angle or control of the ac voltage through tap changing of the converter transformer.

Grid/gate control, which is rapid (1 to 10 ms), and tap changing, which is slow (5 to 6 s per step), are used in a complementary manner. Grid/gate control is used initially for rapid action, followed by tap changing to restore the converter quantities (α for rectifier and γ for inverter) to their normal range.

Power reversal is obtained by reversal of polarity of direct voltages at both ends.

Basis for selection of controls

The following considerations influence the selection of control characteristics:

1. Prevention of large fluctuations in direct current due to variations in ac system voltage.

2. Maintaining direct voltage near rated value.

3. Maintaining power factors at the sending and receiving end that are as high as possible.

4. Prevention of commutation failure in inverters and arc-back in rectifiers using mercury-arc valves.

Rapid control of the converters to prevent large fluctuations in direct current is an important requirement for satisfactory operation of the HVDC link. Referring to Equation 10.33, the line and converter resistances are small; hence, a small change in V_{dor} or V_{doi} causes a large change in I_d. For example, a 25% change in the voltage at either the rectifier or the inverter could cause direct current to change by as much as 100%. This implies that, if both α_r and γ_i are kept constant, the direct current can vary over a wide range for small changes in the alternating voltage magnitude at either end. Such variations are generally unacceptable for satisfactory performance of the power system. In addition, the resulting current may be high enough to damage the valves and other equipment. Therefore, rapid converter control to prevent fluctuations of direct current is essential for proper operation of the system; without such a control, the HVDC system would be impractical.

For a given power transmitted, the direct voltage profile along the line should be close to the rated value. This minimizes the direct current and thereby the line losses.

There are several reasons for maintaining the power factor high:

(a) To keep the rated power of the converter as high as possible for given current and voltage ratings of transformer and valve;

(b) To reduce stresses in the valves;

(c) To minimize losses and current rating of equipment in the ac system to which the converter is connected;

(d) To minimize voltage drops at the ac terminals as loading increases; and

(e) To minimize cost of reactive power supply to the converters.

From Equation 10.23,

$$\begin{aligned}\cos\phi &\approx 0.5[\cos\alpha + \cos(\alpha+\mu)]\\ &\approx 0.5[\cos\gamma + \cos(\gamma+\mu)]\end{aligned}$$

Therefore, to achieve high power factor, α for a rectifier and γ for an inverter should be kept as low as possible.

The rectifier, however, has a *minimum α limit* of about 5° to ensure adequate voltage across the valve before firing. For example, in the case of thyristors, the positive voltage appearing across each thyristor before firing is used to charge the supply circuit providing the firing pulse energy to the thyristor. Therefore, firing cannot occur earlier than about α=5° [10]. Consequently, the rectifier normally operates at a value of α within the range of 15° to 20° so as to leave some room for increasing rectifier voltage to control dc power flow.

In the case of an inverter, it is necessary to maintain a certain minimum extinction angle to avoid commutation failure. It is important to ensure that commutation is completed with sufficient margin to allow for de-ionization before commutating voltage reverses at α=180° or γ=0°. The extinction angle γ is equal to $\beta-\mu$, with the overlap μ depending on I_d and the commutating voltage. Because of the possibility of changes in direct current and alternating voltage even after commutation has begun, sufficient *commutation margin above the minimum γ limit* must be maintained. Typically, the value of γ with acceptable margin is 15° for 50 Hz systems and 18° for 60 Hz systems.

Control characteristics

Ideal characteristics:

In satisfying the basic requirements identified above, the responsibilities for voltage regulation and current regulation are kept distinct and are assigned to separate terminals. Under normal operation, the rectifier maintains constant current (CC), and the inverter operates with *constant extinction angle*[1] (CEA), maintaining adequate commutation margin. The basis for this control philosophy is best explained by using the steady-state voltage-current (*V-I*) characteristics, shown in Figure 10.28. The voltage V_d and the current I_d forming the coordinates may be measured at some common point on the dc line. In Figure 10.28, we have chosen this to be at the rectifier terminal. The rectifier and inverter characteristics are both measured at the rectifier; the inverter characteristic thus includes the voltage drop across the line.

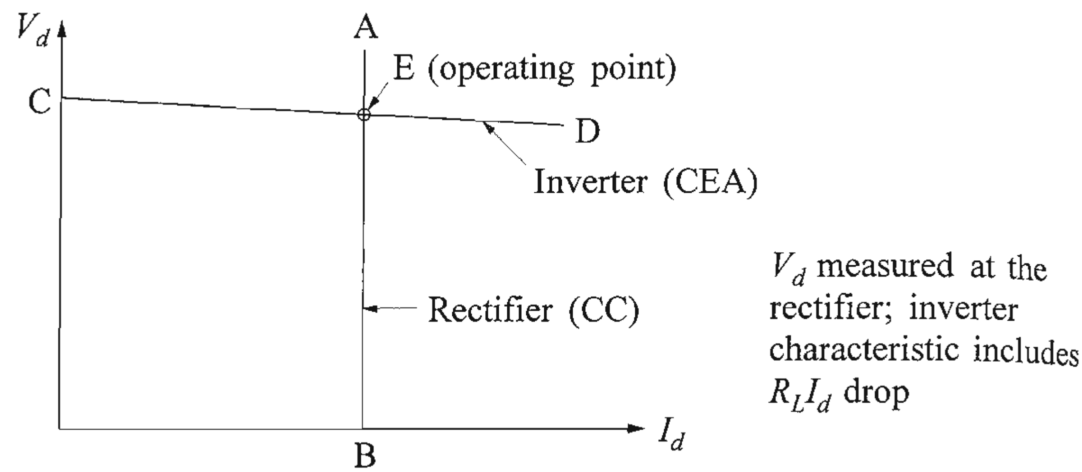


Figure 10.28 Ideal steady-state *V-I* characteristics

With the rectifier maintaining constant current, its *V-I* characteristic, shown as line AB in Figure 10.28, is a vertical line. From Figure 10.27(b),

$$V_d = V_{d0i}\cos\gamma + (R_L - R_{ci})I_d \tag{10.36}$$

This gives the inverter characteristic, with γ maintained at a fixed value. If the commutating resistance R_{ci} is slightly larger than the line resistance R_L, the characteristic of the inverter, shown as line CD in Figure 10.28, has a small negative slope.

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[1] Constant extinction angle control mode is essentially the same as constant margin angle control. Under normal operation, the commutation margin angle and the extinction angles are equal. The distinction arises during conditions such as operation with a large overlap angle; the valve voltage may become positive earlier than when the sinusoidal portion of the voltage would have crossed zero under normal conditions. Under these conditions the concept of maintaining minimum extinction angle is not meaningful. Therefore, the commutation margin angle (representing the interval between the end of conduction and the instant when the actual voltage across the valve becomes positive) is maintained for safe inverter operation.

Since an operating condition has to satisfy both rectifier and inverter characteristics, it is defined by the intersection of the two characteristics (E).

The rectifier characteristic can be shifted horizontally by adjusting the "current command" or "current order." If measured current is less than the command, the regulator advances the firing by decreasing α.

The inverter characteristic can be raised or lowered by means of its transformer tap changer. When the tap changer is moved, the CEA regulator quickly restores the desired γ. As a result, the direct current changes, which is then quickly restored by the current regulator of the rectifier. The rectifier tap changer acts to bring α into the desired range between 10° and 20° to ensure a high power factor and adequate room for control.

To operate the inverter at a constant γ, the valve firing is controlled by a computer which takes into consideration variations in the instantaneous values of voltage and current. The computer controls the firing times so that the extinction angle γ is larger than the de-ionization angle of the valve.

Actual characteristics:

The rectifier maintains constant current by changing α. However, α cannot be less than its minimum value (α_{min}). Once α_{min} is reached, no further voltage increase is possible, and the rectifier will operate at *constant ignition angle* (CIA). Therefore, the rectifier characteristic has really two segments (AB and FA) as shown in Figure 10.29. The segment FA corresponds to minimum ignition angle and represents the CIA control mode; the segment AB represents the normal constant current (CC) control mode.

In practice, the constant current characteristic may not be truly vertical, depending on the current regulator. With a proportional controller, it has a high negative slope due to the finite gain of the current regulator, as shown below.

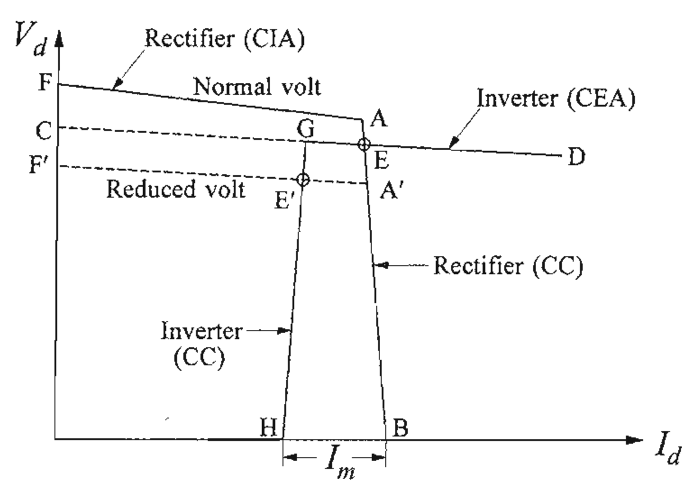


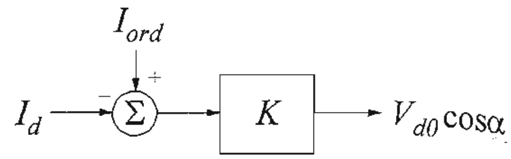
Figure 10.29 Actual converter control steady-state characteristics

With a regulator gain of K, we have

$$V_{d0}\cos\alpha = K(I_{ord} - I_d)$$
$$= V_d + R_{cr} I_d$$

Therefore,

$$V_d = KI_{ord} - (K + R_{cr})I_d$$



I_{ord} = current order

Figure 10.30 Current regulator

In terms of perturbed values,

$$\Delta V_d = -(K+R_{cr})\,\Delta I_d$$

or

$$\Delta V_d / \Delta I_d = -(K+R_{cr}) \tag{10.37}$$

With a proportional plus integral regulator, the CC characteristic is quite vertical. The complete rectifier characteristic at normal voltage is defined by FAB. At a reduced voltage it shifts, as indicated by F′A′B.

The CEA characteristic of the inverter intersects the rectifier characteristic at E for normal voltage. However, the inverter CEA characteristic (CD) does not intersect the rectifier characteristic at a reduced voltage represented by F′A′B. Therefore, a big reduction in rectifier voltage would cause the current and power to be reduced to zero after a short time depending on the dc reactors. The system would thus run down.

In order to avoid the above problem, the inverter is also provided with a current controller, which is set at a lower value than the current setting for the rectifier. The complete inverter characteristic is given by DGH, consisting of two segments: one of CEA and one of constant current.

The difference between the rectifier current order and the inverter current order is called the *current margin*, denoted by I_m in Figure 10.29. It is usually set at 10 to 15% of the rated current so as to ensure that the two constant current characteristics do not cross each other due to errors in measurement or other causes.

Under normal operating conditions (represented by the intersection point E), the rectifier controls the direct current and the inverter the direct voltage. With a reduced rectifier voltage (possibly caused by a nearby fault), the operating condition is represented by the intersection point E′. The inverter takes over current control and the rectifier establishes the voltage. In this operating mode, the roles of the rectifier and inverter are reversed. The change from one mode to another is referred to as a *mode shift*.

Combined rectifier and inverter characteristics

In most HVDC systems, each converter is required to function as a rectifier

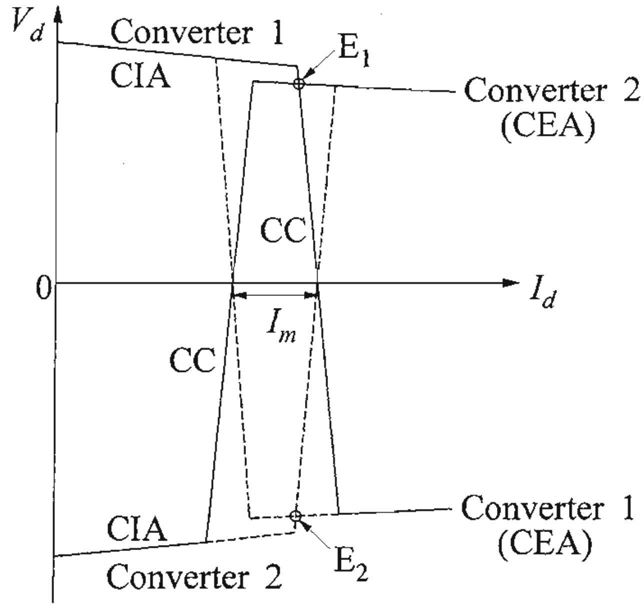


Figure 10.31 Operation with each converter having combined inverter and converter characteristics

as well as an inverter. Consequently, each converter is provided with a combined characteristic as shown in Figure 10.31.

The characteristic of each converter consists of three segments: constant ignition angle (CIA) corresponding to α_{min}, constant current (CC), and constant extinction angle (CEA).

The power transfer is from converter 1 to converter 2, when the characteristics are as shown in Figure 10.31 by solid lines. The operating condition in this mode of operation is represented by point E_1.

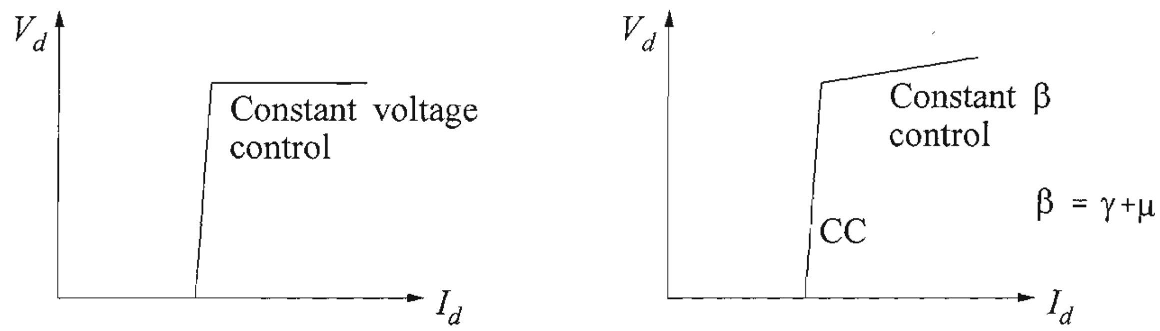
The power flow is reversed when the characteristics are as shown by the dotted lines. This is achieved by reversing the "margin setting," i.e., by making the current order setting of converter 2 exceed that of converter 1. The operating condition is now represented by E_2 in the figure; the current I_d is the same as before, but the voltage polarity has changed.

Alternative inverter control modes

The following are variations to the CEA control mode described above for the inverter. These variations offer some advantages in special cases.

DC voltage control mode:

Instead of regulating to a fixed γ value (CEA), a closed-loop voltage control may be used so as to maintain a constant voltage at a desired point on the dc line, usually the sending end (rectifier). The necessary inverter voltage to maintain the desired dc voltage is estimated by computing the line *RI* drop. As compared to constant γ control (which has drooping voltage characteristic), the voltage control mode has the advantage that the inverter *V-I* characteristic is flat as shown in Figure 10.32(a). In addition, the voltage control mode has a slightly higher value of γ and is thus less prone to commutation failure. Normally the voltage control mode maintains a γ of about 18° in conjunction with the tap changers.



(a) Constant voltage mode (b) Constant β mode

Figure 10.32 Alternative inverter control modes

Beta (β) control:

The inverter equivalent circuit in terms of ignition advance angle β is as shown in Figure 10.21(a). With constant β, the *V-I* characteristic of the inverter therefore has a positive slope as shown in Figure 10.32(b). At low loads, constant β gives additional security against commutation failure. However, at higher currents (larger overlap), the minimum γ may be encountered. Constant β control mode is not used for normal operation. It is viewed as a backup type of control mode useful for acting directly upon the firing angle during transient conditions.

Mode stabilization

As shown in Figure 10.33, the intersection of rectifier α_{min} characteristic and the inverter CEA may not be well defined at certain voltage levels near the transition between the inverter CEA and CC characteristics. In this region, a small change in ac voltage will cause a large (10%) change in direct current. There will also be a tendency to "hunt" between modes and tap changing. In order to avoid this problem, a characteristic with positive slope (constant β) at the transition between CEA and CC control characteristic of the inverter is often provided as shown in Figure 10.34(a). Another variation, shown in Figure 10.34(b), controls the direct voltage with a voltage feedback loop.

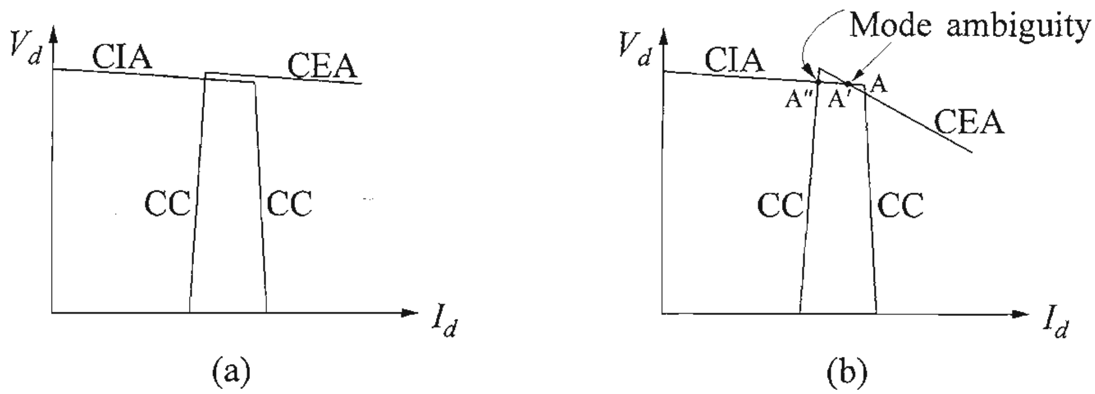


Figure 10.33 Regions of mode ambiguity

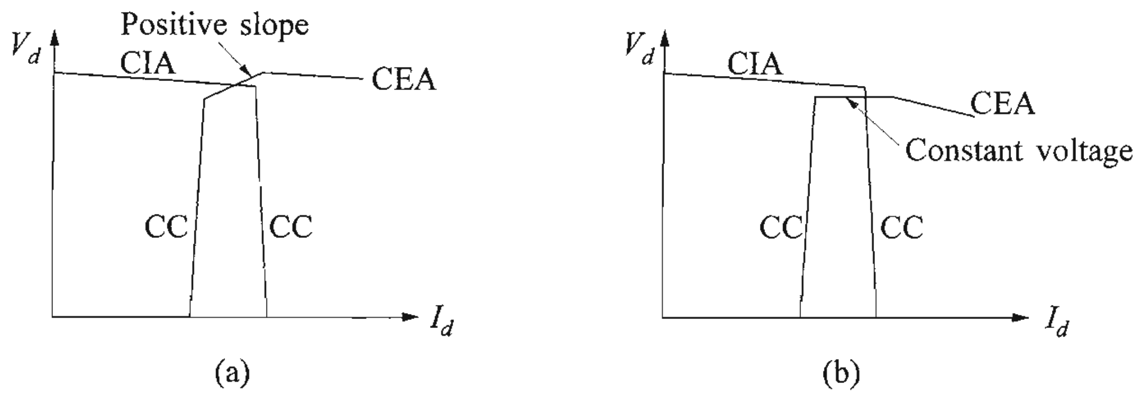


Figure 10.34 Modification of *V-I* characteristic for mode stabilization

Tap changer control

Tap changer control is used to keep the converter firing angles within the desired range, whenever α (for rectifier) or γ (for inverter) exceeds this range for more than a few seconds.

Normally, the inverter operates at constant extinction angle, thus fixing the line voltage with superimposed voltage control by the tap changer. The rectifier operates in current control mode with superimposed $\alpha = \alpha_{nominal}$ control by the tap changer.

Tap changers are usually sized to allow for minimum and maximum steady-state voltage variations, and for minimum to maximum power flow under worst-case steady-state voltage conditions. Unnecessary tap movements during transient conditions are prevented by using time delays. Hunting of the tap changer is avoided by having a dead band wider than the tap-step size.

Current limits

The following limits have to be recognized in establishing the current order.

(a) Maximum current limit:

The maximum short-time current is usually limited to 1.2 to 1.3 times normal full-load current, to avoid thermal damage to valves.

(b) Minimum current limit:

At low values of current, the ripple in the current may cause it to be discontinuous or intermittent. In a 12-pulse operation, the current is then interrupted 12 times per cycle. This is objectionable because of the high voltages (*Ldi/dt*) induced in the transformer windings and the dc reactor by the high rate of change of current at the instants of interruption.

At low values of direct current, the overlap is small. Operation is objectionable even with continuous current if the overlap is too small. With a very small overlap, the two jumps in direct voltage at the beginning and end of commutation merge to form one jump twice as large, resulting in an increased stress on the valves. It may also cause flashover of protective gaps placed across the terminals of each bridge [2].

(c) Voltage-dependent current-order limit[1] *(VDCOL):*

Under low voltage conditions, it may not be desirable or possible to maintain rated direct current or power for the following reasons:

(a) When voltage at one converter drops by more than about 30%, the reactive power demand of the remote converter increases, and this may have an adverse effect on the ac system. A higher α or γ at the remote converter necessary to control the current causes the increase in reactive power. The reduced ac system voltage levels also significantly decrease the reactive power supplied by the filters and capacitors, which often supply much of the reactive power absorbed by the converters.

(b) At reduced voltages, there are also risks of commutation failure and voltage instability.

These problems associated with operation under low-voltage conditions may be prevented by using a "voltage-dependent current-order limit" (VDCOL). This limit reduces the maximum allowable direct current when the voltage drops below a predetermined value. The VDCOL characteristics may be a function of the ac commutating voltage or the dc voltage. The two types of VDCOLs are illustrated in Figure 10.35.

The rectifier inverter static *V-I* characteristics, including VDCOL, are shown in Figure 10.36. The inverter characteristic matches the rectifier VDCOL to preserve the current margin. The general practice is to transiently reduce the current order through voltage-dependent current limit. For VDCOL operation, the measured direct

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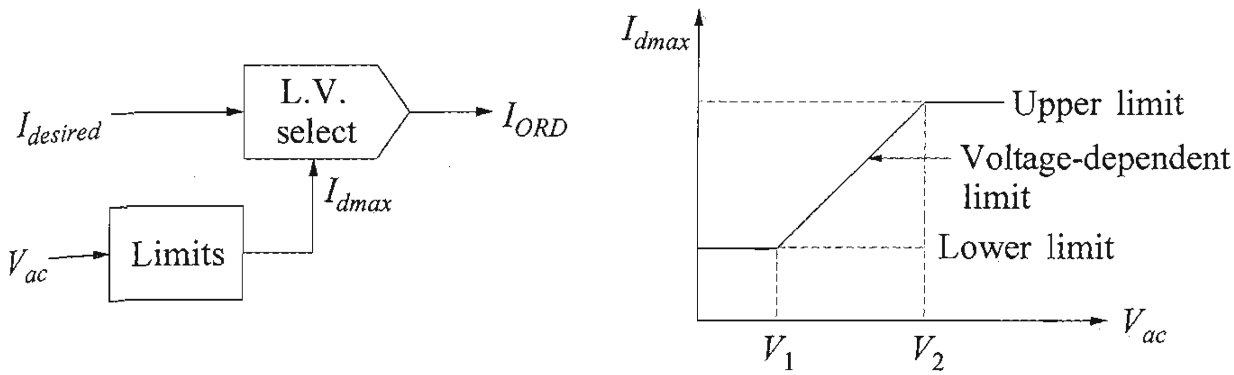
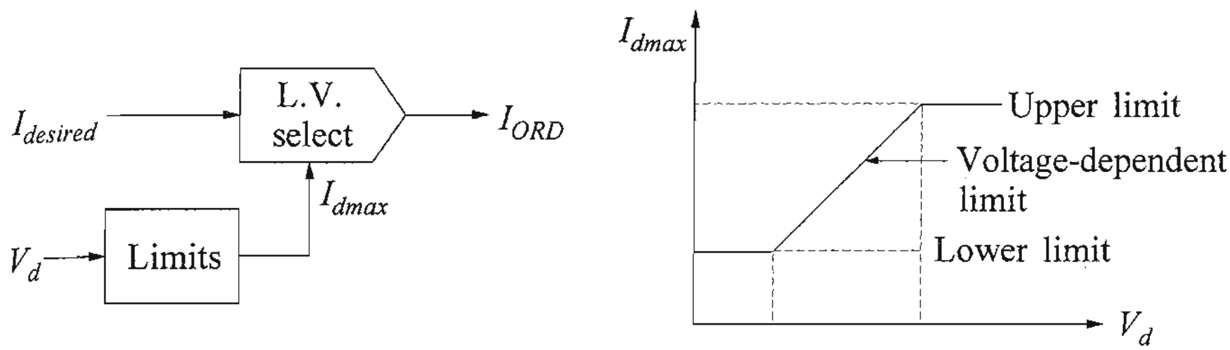
1 This is also referred to as *voltage dependent current limit* (VDCL).



(a) Current limit as a function of alternating voltage



(b) Current limit as a function of direct voltage

Figure 10.35 Voltage-dependent current limits

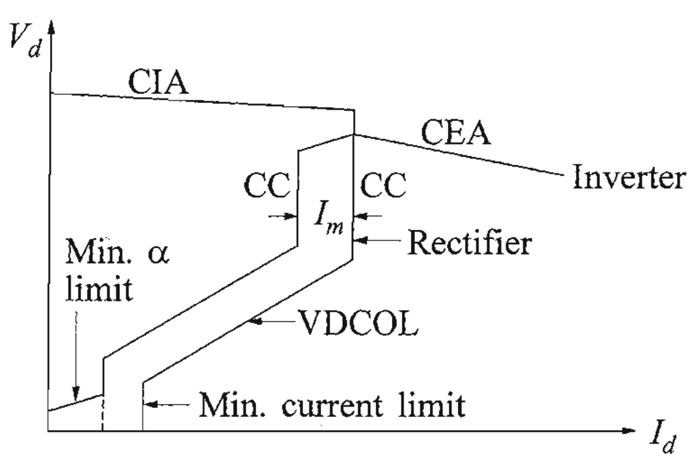


Figure 10.36 Steady-state *V-I* characteristic with VDCOL, minimum current limit and firing angle limits

voltage is passed through a first-order time lag element. Generally, this time lag is different for increasing and decreasing voltage conditions. While the voltage is going down, fast VDCOL action is required; hence, the time lag is small. If the same short time lag is used during voltage recovery, it may lead to oscillations and possibly instability. To prevent this, the larger time lag is used when the direct voltage is recovering.

Minimum firing angle limit

As shown in Figure 10.31, power transfer over the dc line can be controlled by manipulation of current order and current margin. These signals are transmitted to the converter stations through a telecommunication link. In the event that the communication fails or in case of a dc line fault, there is a possibility that the inverter station may switch to the rectification mode. This would result in a reversal of power flow. To prevent this from occurring, the inverter control is provided with a minimum-α limit, as indicated by the lowest portion of the inverter V-I characteristic in Figure 10.36. This restricts the firing angle of the inverter to a value greater than 90°, typically in the range of 95° to 110°. The rectifier is, however, allowed to operate in the inverter region to assist the system under certain fault conditions. As a consequence, the maximum limit imposed on the rectifier firing angle is typically between 90° and 140°.

Power control

Usually, an HVDC link is required to transmit a scheduled power. In such an application, the corresponding current order is determined as being equal to the power order (P_0) divided by the measured direct voltage:

$$I_{ord} = P_0/V_d$$

The current order so computed is used as input signal to the current control. However, high-speed constant power control may have an adverse effect on ac system stability. From the viewpoint of system stability, high-speed constant current control with a superimposed slow power control is preferable. This is acceptable since the dispatcher is not interested in a very high speed power control. Thus, from the stability viewpoint, the HVDC system control performs as a constant current control, but for the dispatcher it appears as constant power control.

Auxiliary controls for ac system

To enhance ac system performance, auxiliary signals derived from the ac system quantities may be used to control the converters. The control strategy could include modulation of either direct current or direct voltage, or both. In addition, special control measures may be used to assist recovery of dc systems from faults. These higher-level controls will be discussed in more detail later in this chapter.

Summary of basic control principles

The HVDC system is basically constant-current controlled for the following two important reasons:

- To limit overcurrent and minimize damage due to faults
- To prevent the system from running down due to fluctuations of the ac voltages

It is because of the high-speed constant current control characteristic that the HVDC system operation is very stable.

The following are the significant aspects of the basic control system:

(a) The rectifier is provided with a *current control* and an *α-limit control.* The minimum α reference is set at about 5° so that sufficient positive voltage across the valve exists at the time of firing, to ensure successful commutation. In the current control mode, a closed-loop regulator controls the firing angle and hence the dc voltage to maintain the direct current equal to the current order. Tap changer control of the converter transformer brings α within the range of 10° to 20°. A time delay is used to prevent unnecessary tap movements during transient excursions of α.

(b) The inverter is provided with a *constant extinction angle* (CEA) control and a *current control.* In the CEA control mode, γ is regulated to a value of about 15°. This value represents a trade-off between acceptable var consumption and a low risk of commutation failure. While CEA control is the norm, there are variations which include *voltage control* and *β control.* Tap changer control is used to bring the value of γ close to the desired range of 15° to 20°.

(c) Under normal conditions, the rectifier is on current control mode and the inverter is on CEA control mode. If there is a reduction in ac voltage at the rectifier end, the rectifier firing angle decreases until it hits the α_{min} limit. At this point, the rectifier switches to α_{min} control and the inverter will assume current control.

(d) To ensure satisfactory operation and equipment safety, several limits are recognized in establishing the current order: maximum current limit, minimum current limit, and voltage-dependent current limit.

(e) Higher-level controls may be used, in addition to the above basic controls, to improve ac/dc system interaction and enhance ac system performance.

All schemes used to date have used the above modes of operation for the rectifier and the inverter. However, there are some situations that may warrant serious investigation of a control scheme in which the inverter is operated continuously in current control mode and the rectifier in α-minimum control mode. Enhanced performance into weak systems may be one case.

10.4.2 Control Implementation

In Section 10.4.1, we considered the basic principles of control of one pole. Figure 10.37 illustrates a general scheme for implementing the controls. In many cases there are two to four converter bridges per pole connected in series. Usually, two bridges with Y-Y and Y-Δ connected transformers are considered as one 12-pulse unit. Thus, the smallest unit to be controlled is a 6-pulse or a 12-pulse bridge unit.

The control hierarchy varies from one dc system to another, but the general concepts are common. Figure 10.38 illustrates the control hierarchy of a typical bipolar HVDC system. The control scheme is divided into four levels: bridge or converter unit control, pole control, master control and overall control.

The *bridge* or *converter unit control* determines the firing instants of the valves within a bridge and defines α_{min} and γ_{min} limits. This has the fastest response within the control hierarchy.

The *pole control* coordinates the control of bridges in a pole. The conversion of current order to a firing angle order, tap changer control, and certain protection sequences are handled by the pole control. This includes coordination of starting up, deblocking, and balancing of bridge controls.

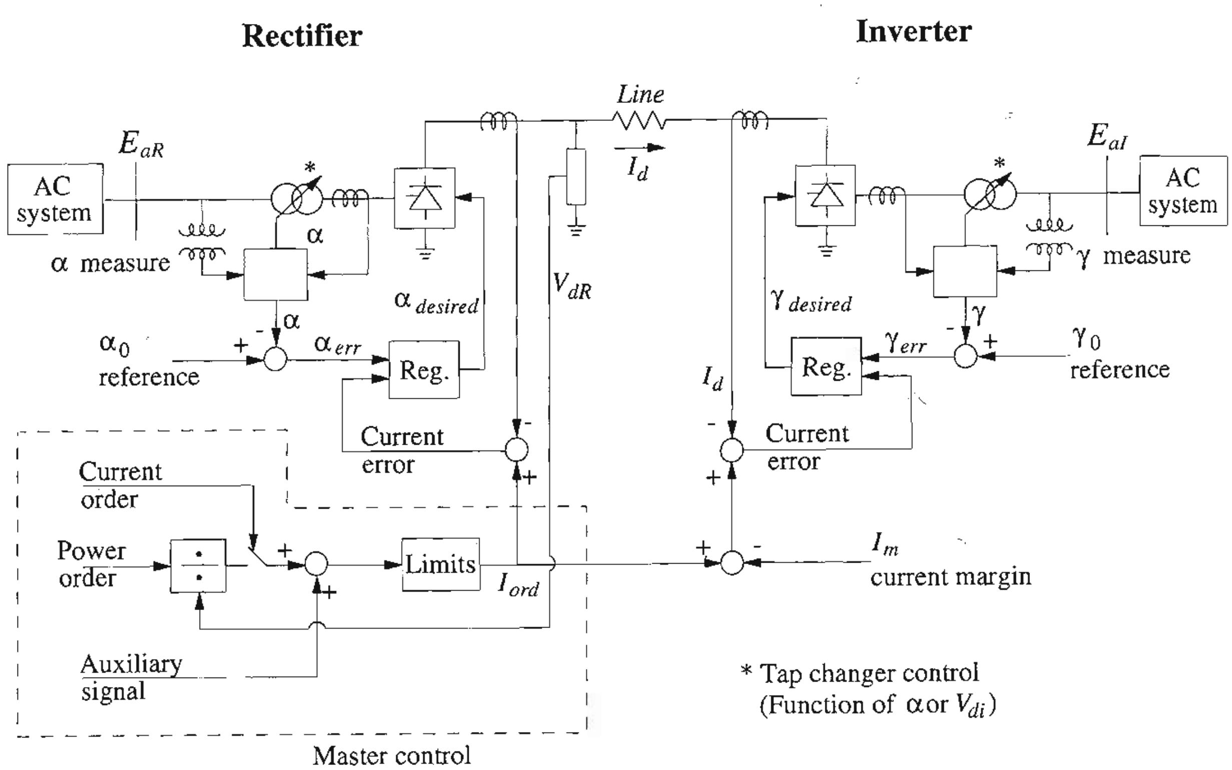


Figure 10.37 Basic control scheme

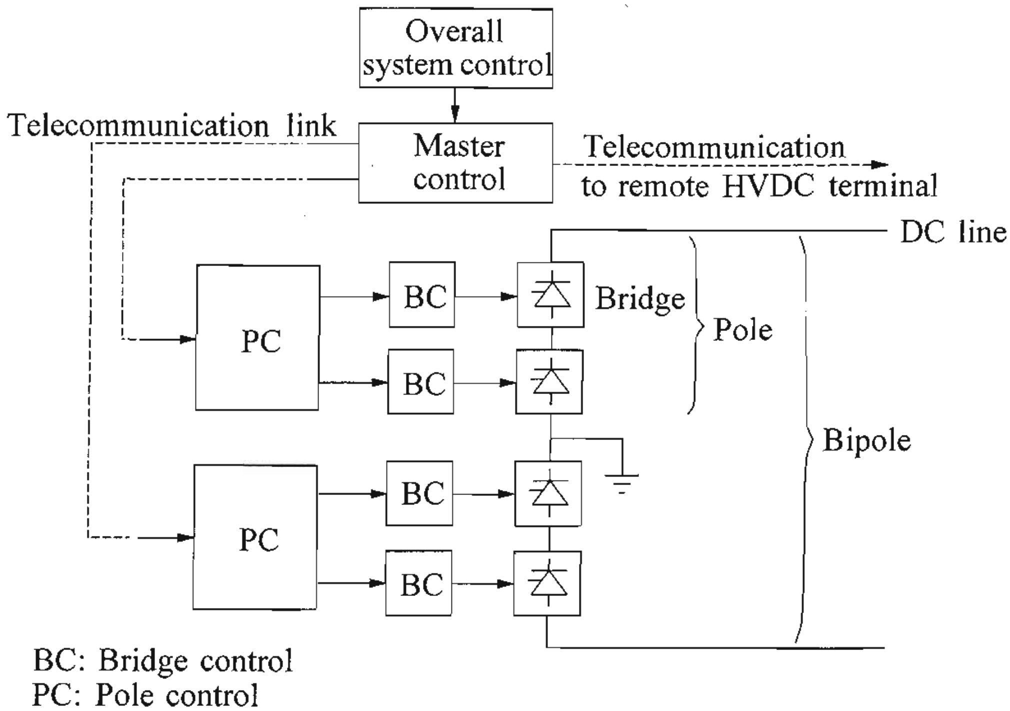


Figure 10.38 Hierarchy of different levels of HVDC system controls

The *master control* determines the current order and provides coordinated current order signals to all the poles. It interprets the broader demands for controlling the HVDC system by providing an interface between pole controls and the *overall system control*. This includes power-flow scheduling determined by the control centre and ac system stabilization.

The basic control functions are similar for most applications. However, higher-level control functions are determined by the specific performance objectives of individual systems. For reliable operation of the HVDC system, each pole should function as independently as possible. The control and protection functions should be segregated and implemented at the lowest possible level of hierarchy.

The control of HVDC systems clearly requires communication between terminals for proper operation. In the case of rapid changes in power level, high-speed communication is required to maintain consistent current settings at the two terminals. Change of power direction requires communication to transfer the current margin setting from one terminal to the other. The starting and stopping of the terminals require coordination of the operations at the two terminals. Communication is also required for transmittal of general status information needed by the operators. Protection may also require communication between the terminals for detection of some faults.

There are several alternative transmission media available for the telecommunications: direct wires via private lines or telephone networks, power-line carrier, microwave systems, and fibre optics. The choice of the telecommunication medium will depend on the amount of information to be transmitted and the required speed of response, degree of security, and noise immunity.

10.4.3 Converter Firing-Control Systems

The converter firing-control system establishes the firing instants for the converter valves so that the converter operates in the required mode of control: constant current (CC), constant ignition angle (CIA), or constant extinction angle (CEA).

Two basic types of controls have been used for the generation of converter firing pulses:

- Individual phase control (IPC)
- Equidistant pulse control (EPC)

The implementation of the above basic forms of converter firing control has evolved over the years. There are several different versions in existence depending on the manufacturer and the vintage of equipment. Their detailed description is beyond the scope of this book. The following descriptions illustrate the principles of operation of the two forms of converter firing-control systems.

Individual phase control system [11,12]

This system was widely used in the early HVDC installations. Its main feature is that the firing pulses are generated individually for each valve, determined by the zero crossing of its commutation voltage.

The commutation process in a three-phase bridge circuit was analyzed in Section 10.2. Referring to Figure 10.15 and Equation 10.7A, the commutation voltage is given by

$$\begin{aligned} e_{ba} &= e_b - e_a \\ &= \sqrt{3}E_m \sin\omega t = 2L_c \frac{di_3}{dt} \end{aligned}$$

As depicted in Figure 10.39, commutation begins when ωt equals the ignition angle (α) and ends when ωt equals the normal extinction angle ($\pi-\gamma$).

If $t=t_1$ at the beginning of commutation, and $t=t_2$ at the end of commutation, we may write

$$\int_{t_1}^{t_2} \sqrt{3}E_m \sin\omega t \, dt = 2L_c \int_0^{I_d} di_3$$

or

$$-\sqrt{3}\frac{E_m}{\omega}(\cos\omega t_2 - \cos\omega t_1) = 2L_c I_d$$

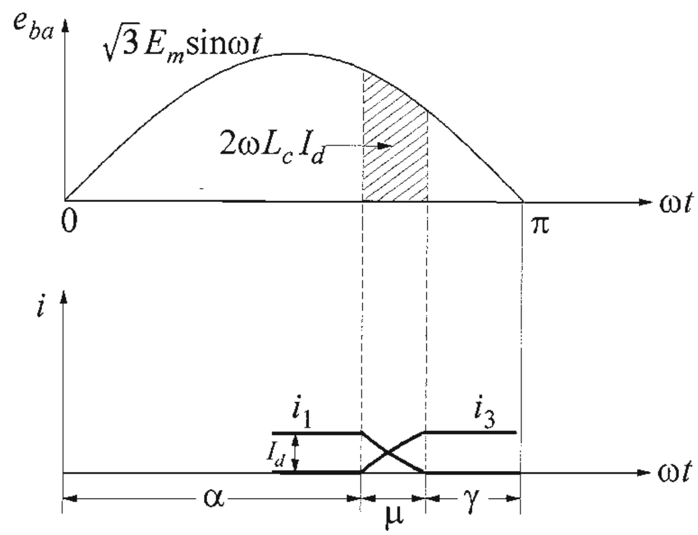


Figure 10.39 Commutation voltage and valve currents

or

$$-\sqrt{3}E_m[\cos(\pi-\gamma)-\cos\omega t_1] = 2\omega L_c I_d$$

Thus the control has to satisfy the condition that the voltage integral $2\omega L_c I_d$ is available between $\omega t=\omega t_1=\alpha$ and $\omega t=\omega t_2=\pi-\gamma$. The equation to be satisfied may be written as

$$-\sqrt{3}E_m\cos\omega t_1-\sqrt{3}E_m\cos\gamma+2X_c I_d = 0 \tag{10.38}$$

CEA control with IPC:

In Equation 10.38, the direct current (I_d) and the commutating voltage vary with changes in operating conditions. The grid control, therefore, senses these two quantities to determine the instant of firing ($t=t_1$) so as to satisfy Equation 10.38. With extinction angle equal to a set value γ_c, and $X_c=\omega L_c$, we have

$$-\sqrt{3}E_m\cos\omega t_1-\sqrt{3}E_m\cos\gamma_c+2X_c I_d = 0 \tag{10.39}$$

The required ignition time t_1 can be found from the solution of Equation 10.39. This is accomplished by using analog circuits in the early converter control applications. The control system consists of three units: the first unit giving a dc output proportional to the direct current I_d; the second giving an output proportional to $E_m\cos\gamma_c$; and the third giving an alternating voltage proportional to the commutating voltage but with a phase lag of 90° (i.e., $E_m\cos\omega t$).

The three outputs are added, and a firing pulse is generated when the sum passes through zero. Under steady-state conditions, such a system controls each valve with constant commutation margin, irrespective of load and voltage variations or unbalance.

Constant current control with IPC:

In this case, an additional signal V_{cc} is added to Equation 10.39 as follows:

$$-\sqrt{3}E_m\cos\omega t_1 - \sqrt{3}E_m\cos\gamma_c + 2X_cI_d + V_{cc} = 0 \qquad (10.40)$$

where

$V_{cc} = K(I_o - I_d)$
I_o = current order
I_d = actual direct line current
K = gain of CC control

The same circuit may be used for both CEA and CC control operations [12]. The error $(I_o - I_d)$ is amplified only when I_d is less than I_o. When I_d is greater than I_o, the amplifier output is clamped to zero, and the converter operates on CEA control. When $(I_o - I_d) > 0$, it operates on constant-current control.

The converter characteristics for the full range of inverter and rectifier operation is shown in Figure 10.40. The realization of CIA control ($\alpha = \alpha_c$) is similar to that of CEA control.

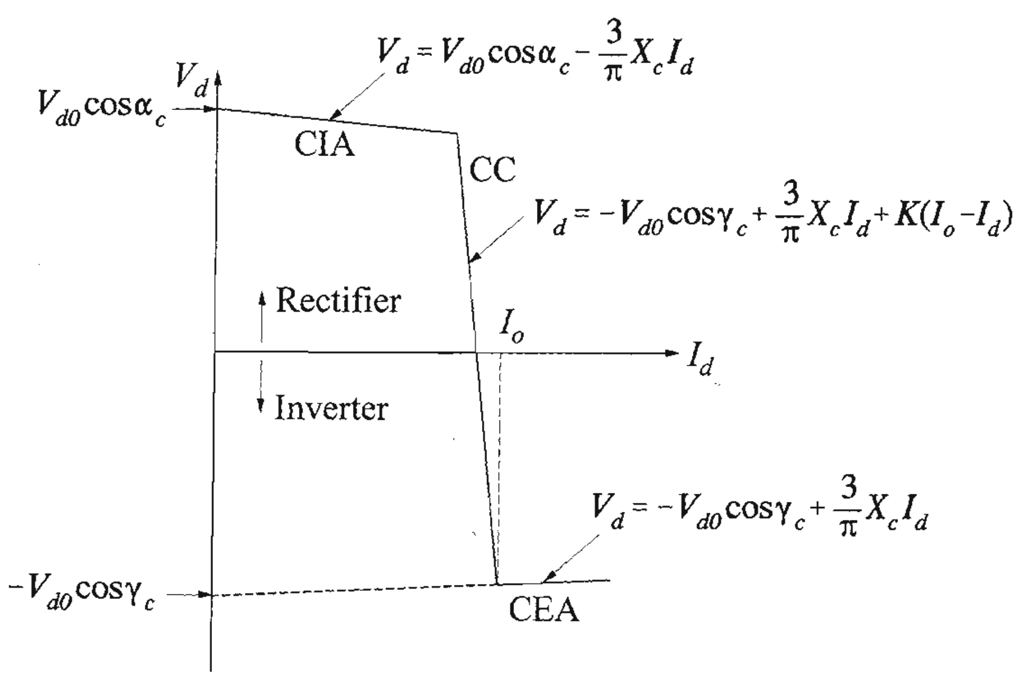


Figure 10.40 Converter characteristics with IPC

The IPC system has the advantage of being able to achieve the highest possible direct voltage under unsymmetrical or distorted supply waveforms since the firing instant for each valve is determined independently. However, the IPC system in effect has a voltage feedback, since the control signal is derived from the alternating line voltage. Any deviation from the ideal voltage waveforms will disturb the symmetry of the current waveforms. This will in turn cause additional waveform distortions, thus introducing non-characteristic harmonics (see Section 10.5). If the ac network to which the converter is connected is weak (i.e., has high impedance), the feedback effect may further distort the altering voltage and thereby lead to harmonic instability.

The harmonic instability problem can be reduced by altering the harmonic characteristics of the ac network (for example, by using additional filters) or adding filters in the control circuit. Alternatively, a firing control system independent of the ac system quantities may be used. This leads to the EPC system described next.

Equidistant pulse control system [10,13]

In this system, valves are ignited at equal time intervals, and the ignition angles of all valves are retarded or advanced equally so as to obtain the desired control mode. There is only indirect synchronization to the ac system voltage.

An EPC system using a phase-locked oscillator to generate the firing pulses was first suggested in reference 13. Since the late 1960s, all manufacturers of HVDC equipment have used this system for converter firing control.

Figure 10.41 shows an EPC-based constant-current control system. The basic components of the system are a voltage-controlled oscillator (VCO) and a ring counter. The VCO delivers pulses at a frequency directly proportional to the input control voltage. The train of pulses is fed to the ring counter, which has six or twelve stages (depending on the pulse number of the converter). Only one stage is on at any time, with the pulse train output of the VCO changing the on stage of the ring counter in cyclic manner. As each stage turns on, it produces a short output pulse once per

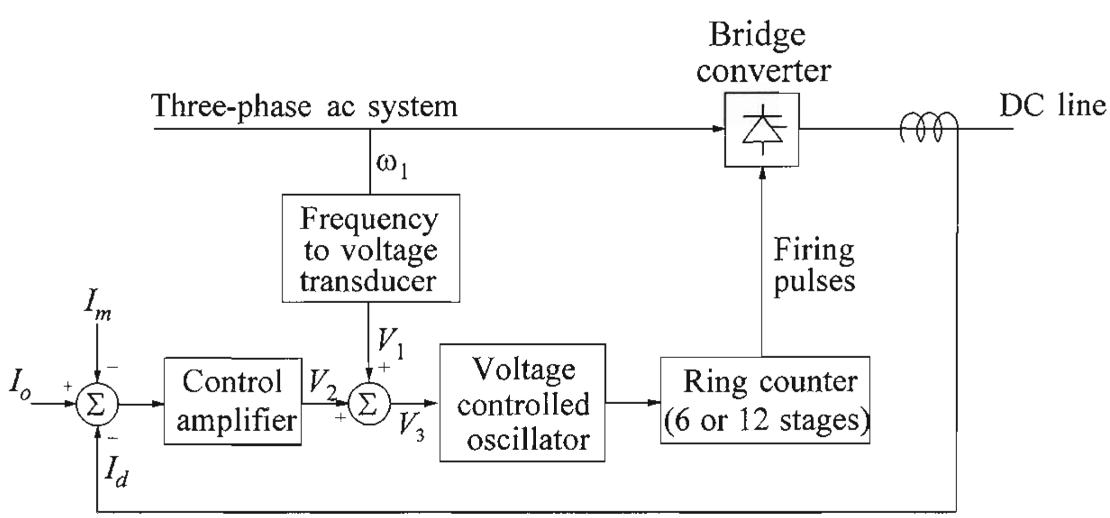


Figure 10.41 Current control system with equidistant pulse control

cycle. Over one full cycle, a complete set of 6 (or 12) output pulses is produced by the ring counter at equal intervals. These pulses are transferred by the firing-pulse generator to the appropriate valves of the converter bridge.

Under steady-state conditions, V_2 is zero and the voltage V_1 is proportional to the ac line frequency ω_1. This generates pulses at line frequency, and maintains a constant firing delay angle α. If there is a change in current order I_o, margin setting I_m, or line frequency ω_1, a change in V_3 occurs which in turn results in a change in the frequency of the firing pulses. A change in firing delay angle ($\Delta\alpha$) results from the *time integral* of the differences between line and firing pulse frequencies. It is apparent that this equidistant pulse control firing scheme is based on pulse frequency control.

An alternative equidistant pulse control firing scheme based on pulse phase control is proposed in reference 14. In this scheme, a step change in control signal causes the spacing of only one pulse to change; this results in a shift of phase only.

For CEA control, the basic circuits of Figure 10.41, illustrated for CC control, must be supplemented by additional circuitry. Since the extinction angle ($\gamma=\pi-\alpha-\mu$) cannot be controlled directly, either a predictive or a feedback control has to be used. In the scheme described in reference 10, a predictive method is used to ensure that adequate commutation voltage-time area (see Figure 10.39) is available at the instant of firing for successful commutation. The firing angle is based on calculation of the overlap angle (μ) from measured values of current and voltage. Reference 13 uses a feedback method to achieve this.

These schemes provide equal pulse spacing in the steady state. Symmetry is maintained relative to the most vulnerable control angle. For example, the smallest γ becomes the set angle in the presence of finite ac voltage unbalance.

The equidistant firing control results in a lower level of non-characteristic harmonics and stable control performance when used with weak ac systems. However, when the ac network asymmetry is large, it results in a lower direct voltage and power than the individual phase control.

Firing system

In modern converters, the valve firing and valve monitoring are provided through an *optical* interface. Light guides are used to carry the firing pulse to each thyristor. Each thyristor is provided with a special control unit that changes a light pulse to an electrical pulse to the gate input on the thyristor. Information about the condition of thyristors, required for protection and supervision of valves, is also transmitted by a light guide system from each thyristor.

At present many manufacturers are developing thyristors that are triggered directly by fibre optics.

10.4.4 Valve Blocking and Bypassing

Valve blocking (stopping) is achieved by interruption of positive pulses to the gates of all the valves in a bridge. However, this may result in overvoltages due to current extinction. In some instances, blocking of the valves at the inverter can lead to continuous conduction through previously conducting phases placing the ac voltage on the dc line and direct current on the converter transformer.

It is, therefore, necessary to bypass the bridge when the valves are blocked. This is achieved by using a bypass valve and bypass switch, as shown in Figure 10.42.

The valve currents are commutated into the bypass valve and then the bypass switch is closed to relieve the bypass valve from carrying current continuously.

Bypass pair operation

In converters using thyristors, the use of a separate bypass valve per bridge has been discontinued. Instead, as shown in Figure 10.43, bypass is implemented by firing a valve to establish a series pair on the same phase as an already conducting valve. A bypass switch closes to relieve the valves during a sustained blocking.

The logic for bypass operation is made part of the converter control.

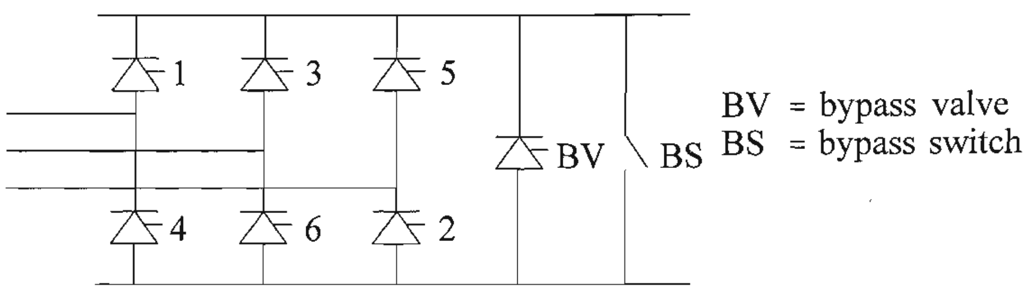


Figure 10.42

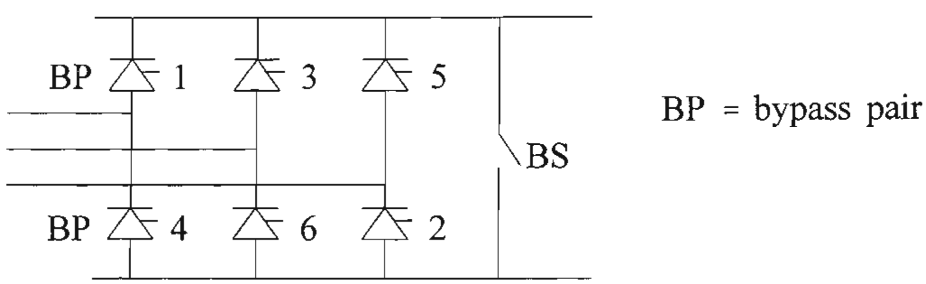


Figure 10.43

10.4.5 Starting, Stopping, and Power-Flow Reversal

The sequences that are used for starting and stopping HVDC systems vary depending on the manufacturer and equipment capability. The rate of rise of voltage, current, and power is tailored to the individual application. The following are typical steps and procedures involved [15].

Normal starting (deblocking) sequence

1. Either the inverter or the rectifier may start first. The converter that is started first establishes valve firing and conduction. Voltage is held low with the deblocking firing angle being in the range of 60° to 70°.

2. Following a communication delay, the other converter also establishes firing. A fairly low voltage is maintained with a firing angle of 60° to 70° and a starting current on the order of 0.2 to 0.3 pu (optimized to equipment or system conditions) is circulated.

3. After a successful start has been established, voltages are increased according to the relaxation rate on firing angle (α or β). The initial current order of 0.2 to 0.3 pu is maintained until the voltage has reached a setpoint of 40% to 80%. The current order is then released to the desired value.

4. When the current is established and can be maintained by the rectifier, the inverter goes into voltage/margin angle control mode.

The entire procedure can take as short a time as a fraction of a second or as long as several minutes, depending on the power order and limitations imposed by the ac system. The load may be increased exponentially or in small steps.

Normal stopping (blocking) sequence

Unlike in ac systems where a circuit-breaker is operated to isolate a line, the dc link is shut down gradually through controls. The blocking of a pole is achieved by reducing the voltage and current to zero as follows:

1. The current and voltage are ramped down within 100 to 300 ms. Then the rectifier is operated in or near the inverter region. This removes any stored energy from the dc system.

2 Bypass switches, if provided, are closed.

If one of two valve groups is to be blocked, it cannot involve reduction of current flow to zero. Therefore, the firing angle of the valve group is ramped to 90°, a bypass is formed with a bypass switch, and the valves are blocked. The ramp rate may be limited to avoid regulator mode changes.

Reversal of power flow

HVDC systems are inherently capable of power flow in either direction. Most schemes have full control features that permit bidirectional power flow.

Power reversal can be smoothly executed by following a prescribed series of ramps or it can be very fast with or without blocking of the firing of the valves.

Control techniques for power reversal may include the following [15]:

1. Reduction of current to 0.1 to 0.5 pu via a step or ramp.

2. Decrease/increase of voltage via ramp or exponential function followed by a current ramp to reach the required level.

The basis for deciding the sequence to be followed is normally the ability of the ac system to survive the resulting disturbance and the need for power reversal within a specified time. Typically, fast power reversal times would be on the order of 20 to 30 ms, although ac system limitations, dc cable design constraints, or power dispatch conditions may increase it to several seconds. HVDC controls can meet this entire range of requirements.

10.4.6 Controls for Enhancement of AC System Performance

In a dc transmission system, the basic controlled quantity is the direct current, controlled by the action of the rectifier with the direct voltage maintained by the inverter. A dc link controlled in this manner buffers one ac system from disturbances on the other. However, it does not allow the flow of synchronizing power which assists in maintaining stability of the ac systems. The converters in effect appear to the ac systems as frequency-insensitive loads and this may contribute to negative damping of system swings. Further, the dc links may contribute to voltage collapse during swings by drawing excessive reactive power.

Supplementary controls are therefore often required to exploit the controllability of dc links for enhancing the ac system dynamic performance. There are a variety of such higher level controls used in practice. Their performance objectives vary depending on the characteristics of the associated ac systems. The following are the major reasons for using supplementary control of dc links:

- Improvement of damping of ac system electromechanical oscillations.
- Improvement of transient stability.
- Isolation of system disturbance.
- Frequency control of small isolated systems.
- Reactive power regulation and dynamic voltage support.

References 18 to 21 provide descriptions of supplementary controls used in a number of HVDC transmission systems for enhancement of ac system performance. The controls used tend to be unique to each system. To date, no attempt has been made to develop generalized control schemes applicable to all systems.

The supplementary controls use signals derived from the ac systems to modulate the dc quantities. The modulating signals can be frequency, voltage magnitude and angle, and line flows. The particular choice depends on the system characteristics and the desired results.

The principles of dc modulation schemes and details of their application for enhancement of ac system performance are discussed further in Chapter 17.

10.5 HARMONICS AND FILTERS

Converters generate harmonic voltages and currents on both ac and dc sides. In this section we will briefly describe the types of harmonics produced by the converters and the characteristics of filters used to minimize their adverse effects.

10.5.1 AC Side Harmonics

Figure 10.12 shows the wave shape of the alternating current under the "ideal" condition with no commutation overlap, ripple-free direct current, balanced purely sinusoidal commutating voltages, and equally-spaced converter firing pulses. The current may be expressed as a Fourier series.

For a 6-pulse bridge with Y-Y transformer connection, the Fourier series expansion for the alternating current is

$$i = \frac{2\sqrt{3}}{\pi}I_d\left(\sin\omega t - \frac{1}{5}\sin 5\omega t - \frac{1}{7}\sin 7\omega t + \frac{1}{11}\sin 11\omega t + \frac{1}{13}\sin 13\omega t - \cdots\right) \qquad (10.41)$$

For a Δ-Y transformer connection, the current is

$$i = \frac{2\sqrt{3}}{\pi}I_d\left(\sin\omega t + \frac{1}{5}\sin 5\omega t + \frac{1}{7}\sin 7\omega t + \frac{1}{11}\sin 11\omega t + \frac{1}{13}\sin 13\omega t + \cdots\right) \qquad (10.42)$$

The second harmonic and all even harmonics are absent in the above because there are two current pulses of equal size and opposite polarity per cycle. Since the current pulse width is one-third of a cycle, third and all triple-n harmonics are also absent. The remaining harmonics are on the order of $6n\pm1$, where n is any positive integer.

In a 12-pulse bridge, there are two 6-pulse bridges with two transformers, one with Y-Y connection and the other with Y-Δ connection (see Figure 10.23). The harmonics of odd values of n cancel out. Hence,

$$i = \frac{2\sqrt{3}}{\pi}2I_d(\sin\omega t + \frac{1}{11}\sin 11\omega t + \frac{1}{13}\sin 13\omega t + \frac{1}{23}\sin 23\omega t + \frac{1}{25}\sin 25\omega t + \cdots) \quad (10.43)$$

The remaining harmonics which have the order $12n \pm 1$ (i.e., 11^{th}, 13^{th}, 23^{th}, 25^{th}, etc.) flow into the ac system. Their magnitudes decrease with increasing order; an h^{th} order harmonic has magnitude $1/h$ times the fundamental.

When the commutating reactance is considered, the overlap angle during commutation rounds off the square edges of the current waves, and this reduces the magnitude of harmonic components. The reduction factor of the harmonic components is given by [3]

$$\frac{i_h}{i_{ho}} = \frac{\sqrt{H^2 + K^2 - 2HK\cos(2\alpha + \mu)}}{\cos\alpha - \cos(\alpha + \mu)} \quad (10.44)$$

where

i_h = harmonic current
i_{h0} = harmonic current with no overlap
h = harmonic order
H = $[\sin(h+1)\mu/2]/(h+1)$
K = $[\sin(h-1)\mu/2]/(h-1)$

It is apparent that the harmonics produced on the ac system are a function of the operating conditions. As μ increases, the harmonic component decreases, with the reduction being more pronounced at higher harmonics. Under typical full load conditions, μ is about 20° and α is about 15°; the 11^{th} and 13^{th} harmonics are about 30 to 40% of those shown in the basic equations, which neglected overlap. During faults, however, α reaches nearly 90°, the overlap angle is reduced, and for a given line current the ac harmonics will increase.

The above discussions consider only balanced conditions. The harmonics produced under such ideal conditions are referred to as "characteristic harmonics."

Various unbalances, such as non-equally spaced firing pulses, bus voltage unbalances and unbalances in the commutating reactance between phases will produce additional harmonics which are referred to as "non-characteristic harmonics." Transformer excitation current also contributes to these harmonics.

The converter manufacturers attempt to minimize these harmonics in the design of the terminals. With modern day equal-spaced firing, the biggest sources of non-characteristic harmonics are bus voltage unbalance, transformer impedance unbalance and the transformer excitation current. Unbalances in ac system voltages depend on the operating conditions and are determined by the design and operating practices of the system. Unbalances in the reactances between the phases of the transformer are usually less than 1% of the phase values. With bus voltage unbalance of less than 1% and normal excitation current levels, non-characteristic harmonics are not significant, unless a resonant condition exists at a particular harmonic frequency.

AC harmonic filters

Harmonics have to be filtered out sufficiently at the terminal so that the harmonics entering the ac system are small and distortion of the ac voltage caused by the harmonic currents is within limits. Harmonics, if not reduced by filters, can produce undesirable effects such as telephone interference, higher losses and heating in ac equipment (machines, capacitors, etc.), or resonance problems which could produce overvoltages and/or overcurrents.

The penetration of the harmonics into the ac system and resonance conditions depends on the harmonic impedance of the ac network, which is difficult to determine. It is constantly varying as the circuits are being added or switched out and the system operating conditions are varying. In filter design, quite elaborate studies are undertaken that consider various factors including possible system resonance conditions.

A typical filter system for a 12-pulse converter terminal is shown in Figure 10.44. The filter impedance is minimum at the 11th and 13th harmonics resulting from the two series-resonant tuned branches. The high pass filter maintains a low impedance for higher harmonic frequencies.

Part of the capacitors required for reactive power compensation is provided by filters. The additional cost of converting the required reactive power capacitors to filters is not very high. Of the 50% reactive power compensation required, about 30% would be in filter form divided among the eleventh, thirteenth, and high pass filters.

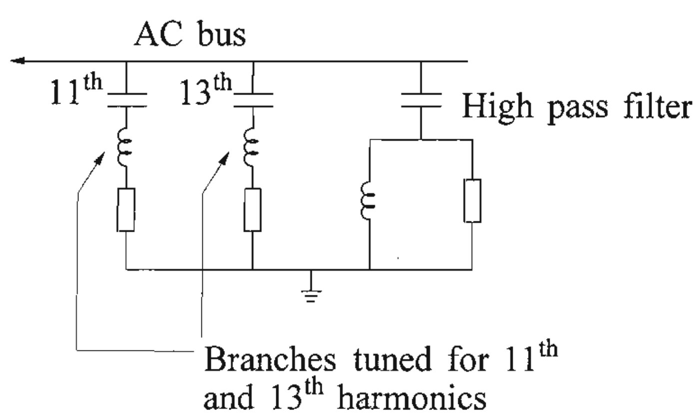


Figure 10.44 Typical filter system configuration

10.5.2 DC Side Harmonics

An ideal 6-pulse bridge converter, with repetitive switching every 60°, produces a direct voltage waveform as shown in Figure 10.19. Fourier analysis of the voltage waveform shows that it contains harmonics of order $6n$ (i.e., 6^{th}, 12^{th}, 18^{th}, etc.). The magnitude of the effective harmonic voltage varies widely over the operating range of α; operation at α near 90° produces higher levels of harmonics than at smaller values of α. The overlap angle μ also has a significant impact on the magnitude of the harmonics.

In a bipole system consisting of two 6-pulse bridges (one in each pole), the transformers would be connected Y-Y and Δ-Y because the 30° phase shift produces cancellation of low order harmonic on the ac bus. This would also have a beneficial effect on the dc side. The 6^{th}, 18^{th}, 30^{th}, ... harmonics are out-of-phase in the two bridges, while the 12^{th}, 24^{th}, 36^{th}, ... harmonics are in phase. The out-of-phase harmonic voltages produce ground return mode currents in the dc line, whereas the in-phase components of harmonic voltages produce line-to-line mode currents.

In the case of a 12-pulse bridge, the out-of-phase components of harmonic voltages will cancel within a 12-pulse bridge; only the in-phase components will produce harmonic currents in the line. For a balanced condition, the significant harmonics in the voltage produced by a dc terminal are therefore of order 12 and its integral multiples.

The non-characteristic harmonics due to unbalances would be small in a well designed system. The dc side harmonics are reduced by the smoothing reactor and filters. Most of the harmonic voltages are dropped across the smoothing reactor. The dc filters are designed to shunt a major portion of the direct harmonic currents so that harmonic currents flowing into the dc line are within the permissible limits.

The smoothing reactor and the rest of the dc system beyond the reactor (dc filters, dc line and remote terminals) act as voltage dividers for the harmonic voltages. In general, a larger value of smoothing reactor will require less dc filtering. However, the smoothing reactor size is influenced by other considerations associated with converter terminal design.

The following are some of the considerations influencing the selection of the smoothing reactor size:

1. The size of the smoothing reactor has a dominant effect on the ripple in the bridge current; the ripple current is less for higher values of the reactor. As discussed in Section 10.4.1, the ripple current determines the minimum current operating point for the terminal.

2. The smoothing reactor, filters, and dc lines combine to produce an impedance to the dc bridge which can be resonant at some generated voltage harmonics. Generally, this is not a problem for the higher harmonics (12^{th}, 24^{th}, ...), but the non-characteristic harmonics generated at low frequency (2^{nd}, 4^{th}, 6^{th}, ...) can produce high harmonic currents if the effective impedance is low at these

frequencies. The high harmonic currents at low frequencies can cause problems with control circuitry and interference with communication circuits. Therefore, the smoothing reactor is selected to avoid a low impedance at 2^{nd} or 4^{th} harmonic frequency. In addition, low frequency harmonic resonance must be avoided for other reasons. Repeated commutation failures on an inverter may introduce fundamental frequency pulses on the dc line (see Section 10.3.2). If the input impedance affecting the bridge were near resonance at the fundamental frequency, high transient voltages would occur.

3. The smoothing reactor size has an influence on the likelihood of commutation failures during a dip in ac voltages and on the likelihood of consequent commutation failure.

4. A higher smoothing reactor limits the fault current near the rectifier.

10.6 INFLUENCE OF AC SYSTEM STRENGTH ON AC/DC SYSTEM INTERACTION

The nature of ac/dc system interactions and the associated problems are very much dependent on the strength of the ac system relative to the capacity of the dc link. The ac system can be considered as "weak" from two aspects: (a) ac system impedance may be high, (b) ac system mechanical inertia may be low [18]. In this section we will discuss problems associated with dc systems connected to weak ac systems and methods of dealing with such problems.

10.6.1 Short-Circuit Ratio

Since the ac system strength has a very significant impact in the ac/dc system interactions, it is useful to have a simple means of measuring and comparing relative strengths of ac systems. The *short-circuit ratio* (SCR) has evolved as such a measure. It is defined as

$$\text{SCR} = \frac{\text{short-circuit MVA of ac system}}{\text{dc converter MW rating}}$$

The short-circuit MVA is given by

$$\text{SC MVA} = \frac{E_{ac}^2}{Z_{th}}$$

where E_{ac} is the commutation bus voltage at rated dc power and Z_{th} is the Thevenin equivalent impedance of the ac system.

The basic SCR gives the inherent strength of the ac system. From the viewpoint of the HVDC system performance, it is more meaningful to consider the *effective short-circuit ratio* (ESCR), which includes the effects of ac side equipment associated with the dc link: filters, shunt capacitors, synchronous condensers, etc.

HVDC controls play an important role in most ac/dc system interaction phenomena, and must be taken into consideration in assessing acceptable levels of ac system strength. Traditionally, the ac system strength has been classified as follows [16]:

- High, if ESCR is greater than 5;
- Moderate, if ESCR is between 3 and 5; and
- Low, if ESCR is less than 3

With refinements in dc and ac system controls, these classifications change. Reference 18 recommends the following classification:

- High, if ESCR is greater than 3;
- Low, if ESCR is between 2 and 3; and
- Very low, if ESCR is less than 2.

The above classification of ac system strength provides a means for preliminary assessment of potential ac/dc interaction problems. Detailed studies are, however, necessary for proper evaluation of the problems. In addition to the short-circuit ratio, the phase angle of the Thevenin equivalent impedance Z_{th} has an impact on the ac/dc system interaction. It is termed the "damping angle" and has an impact on the dc system control stability. Local resistive loads, while not having a significant effect on ESCR, improve damping of the system. Typical values of the damping angle are in the range of 75° to 85°.

10.6.2 Reactive Power and AC System Strength

From Equations 10.12 and 10.25, we have

$$\cos\phi \approx \cos\alpha - \frac{I_d}{V_{d0}}\frac{3}{\pi}X_c$$

Therefore, each converter consumes reactive power which increases with increased power. With normally accepted rectifier ignition delay angle (α) and inverter extinction advance angle (γ) of 15° to 18° and commutating reactance (X_c) of 15%, a converter consumes 50 to 60% reactive power (i.e., if P_{dc}=1.0 pu, Q absorbed by each converter is 0.5 to 0.6 pu). Generally, this has to be provided at the converter site to prevent large reactive power flow through ac lines. Part of the reactive power required is provided by the capacitors associated with the ac filter banks.

The least expensive way to provide the required reactive power is to use shunt capacitor banks. Since the reactive power varies with the dc power transmitted, capacitors must be provided in appropriate sizes of switchable banks, so that steady-state ac voltage is held within an acceptable range (usually ±5%) at all load levels. This is also influenced by the strength of the ac system. The stronger the ac system, the larger the switchable bank size can be for an acceptable voltage change.

Generators, if present near the dc terminal, can be very helpful in handling some of the reactive power demands and in maintaining steady-state voltage within an acceptable range. For weak ac systems, it may be necessary to provide reactive compensation in the form of *static var compensators* (SVCs) or synchronous condensers.

10.6.3 Problems with Low ESCR Systems [16-18]

The following are the problems associated with the operation of a dc system when connected to a weak ac system:

- High dynamic overvoltages,
- Voltage instability,
- Harmonic resonance, and
- Objectionable voltage flicker.

Dynamic overvoltage

When there is an interruption to the dc power transfer, the reactive power absorption of the HVDC converters drops to zero. With a low ESCR system, the resulting increase in alternating voltage due to shunt capacitors and harmonic filters could be excessive. This will require a high insulation level of terminal equipment, thus imposing an economic penalty. It may also cause damage of local customer equipment. Special schemes may be necessary to protect the thyristors in case of restart delays [17].

Voltage stability [16]

With dc systems connected to weak ac systems, particularly on the inverter side, the alternating as well as direct voltages are very sensitive to changes in loading.

An increase in direct current is accompanied by a fall of alternating voltage. Consequently, the actual increase in power may be small or negligible. Control of voltage and recovery from disturbances become difficult. The dc system response may even contribute to collapse of the ac system. The sensitivities increase with large amounts of shunt capacitors.

In such a system, the dc system controls may contribute to voltage instability by responding to a reduction in alternating voltage as follows:

- Power control increases direct current to restore power.
- Inverter γ may increase to maintain volt-second commutation margin.
- Inverter draws more VARs; with reduced voltage, shunt capacitors, however, produce fewer VARs.
- The alternating voltage is reduced, further aggravating the situation.

The process thus leads to progressive fall of voltage.

Harmonic resonance

Most of the problems of harmonic resonance are due to parallel resonance between ac capacitors, filters, and the ac system at lower harmonics.

Capacitors tend to lower the natural resonant frequencies of the ac system, while inductive elements (machines and lines) tend to increase the frequencies. If large numbers of capacitors are added, the natural frequency seen by the commutation bus may drop to 4^{th}, 3^{rd} or even 2^{nd} harmonic. If a resonance at one of these frequencies occurs, there can be a high impedance parallel resonance between the inductive elements and capacitive elements on the commutation bus. A low-impedance series resonance condition could arise in remote points in the system. Harmonic voltages from remote points would tend to be amplified. The avoidance of low-order harmonic resonance is extremely important to reduce transient overvoltages.

Voltage flicker

Another characteristic of a weak ac system is that switching of shunt capacitors and reactors causes unacceptably large voltage changes in the vicinity of compensation equipment. The transient voltage flicker due to frequently switched reactive devices increases with higher levels of dc power transfer.

10.6.4 Solutions to Problems Associated with Weak Systems

The traditional approach to the solution of weak system ac/dc interaction problems is to use synchronous condensers or SVCs. In addition, HVDC controls which switch to current control from power control and reduce direct current for low alternating voltage (for example, VDCOL) will help the situation.

The use of synchronous condensers also reduces the effective system impedance and hence shifts the parallel resonance frequency to higher frequencies at which the system damping is usually better. With 12-pulse bridge circuits, there are no large filters below 11^{th} harmonic; the possibility of excitation of parallel resonance at lower harmonics is therefore low.

An alternative solution to the reactive power and voltage problem is to control the dc converter itself so that the reactive power is modulated in response to voltage variations in a manner similar to an SVC. The shunt capacitors and filters provide the required reactive power; the converter firing angle control stabilizes the ac voltage. Artificial or forced commutation, discussed in Section 10.6.6, provides considerably more freedom in controlling reactive power.

Reference 17 describes five dc links (all back-to-back) connected to weak ac systems, and special techniques used to achieve their satisfactory performance.

10.6.5 Effective Inertia Constant

The ability of the ac system to maintain the required voltage and frequency depends on the rotational inertia of the ac system. For satisfactory performance, the ac system should have a minimum inertia relative to the size of the dc links. A measure of the relative rotational inertia is the effective dc inertia constant, defined as follows [18]:

$$H_{dc} = \frac{\text{total rotational inertia of ac system, MW·s}}{\text{MW rating of dc link}}$$

An effective inertia constant, H_{dc}, of at least 2.0 to 3.0 s is required for satisfactory operation.

For ac systems with very low or no generation, synchronous condensers have to be used to increase the inertia and assist in satisfactory operation of line commutated inverters.

10.6.6 Forced Commutation

The converter bridge circuits we have discussed so far rely on the natural voltage of the ac system for commutation. Such a commutation is known as "natural commutation," and requires the ignition angle (α) to be in the range of 0° to 180° (2° to 165° in practice for reliable turn-on and turn-off of the valves) for successful commutation. As a consequence, the converter absorbs reactive power from the ac system, while operating as a rectifier as well as an inverter.

If our objective is to have the converters supply reactive power to the ac system when so desired, we need to be able to force commutation at any desired point on the ac cycle. This can be achieved by superimposing harmonics or by use of special capacitor circuits to modify the voltages across the valves appropriately in relation to ac system voltages. Such a commutation is called "forced commutation." A system using this form of commutation will also allow feeding into a system without any generation.

A converter bridge circuit with a forced commutation scheme is shown in Figure 10.45 [3,5]. Forced commutation is initiated at the desired times by firing the auxiliary valves (A1 to A6) with the associated capacitors pre-charged. Such capacitive commutations, however, cause considerable stress on the valves and other converter equipment.

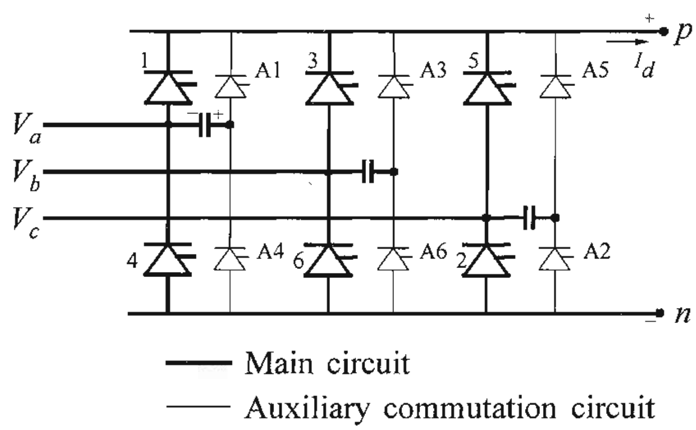


Figure 10.45 Bridge circuit with forced commutation

While converter circuits with forced commutation are feasible, they are very expensive. To date they have not found application in commercial HVDC converters.

Self-commutated voltage sourced inverters using gate turn-off (GTO) thyristors have been used in industrial applications, for example, variable speed drives, uninterruptible power supplies, and battery systems. The voltage and current ratings of these devices are increasing. It is likely that their application for HVDC transmission will become economically practical in the future.

10.7 RESPONSES TO DC AND AC SYSTEM FAULTS

The operation of HVDC transmission is affected by faults on the dc line, converters, or the ac system. The impact of the fault is reflected through the action of converter controls. In ac systems, relays and circuit-breakers are used to detect and remove faults. In contrast, most faults associated with dc systems either are self-clearing or are cleared through action of converter controls. Only in some cases is it necessary to take a bridge or an entire pole out of service. The converter controls thus play a vital role in the satisfactory response of HVDC systems to faults on the dc as well as the ac systems.

10.7.1 DC Line Faults

Faults on dc lines are almost always pole-to-ground faults. A pole-to-pole fault is uncommon since it requires considerable physical damage to bring conductors of two poles together. Lightning never causes a bipolar fault [7].

A pole-to-ground fault blocks power transfer on that pole; the remaining pole is virtually unaffected. As discussed below, the impact of a dc line fault on the connected ac systems is not as disruptive as that of ac faults.

Response of normal control action [2]

A short-circuit momentarily causes the rectifier current to increase (since the rectifier is feeding a low impedance fault rather than the high back voltage of the inverter) and the inverter current to decrease.

The current control of the rectifier acts to reduce the direct voltage and bring back the current to its normal set value (I_{ord}). At the inverter, the current becomes less than its current controller reference setting (I_{ord}–I_m). Consequently, the inverter mode of operation changes from CEA control to CC control. This causes the inverter voltage to run down to zero and then reverse polarity as shown by curve 2 of Figure 10.46. The voltages are equal to the *RI* drop in the line from each converter to the fault. The rectifier current is I_{ord} and inverter current is I_{ord}–I_m in the opposite direction. The steady-state fault current is thus equal to the current margin I_m, which is only about 15% of the rated current.

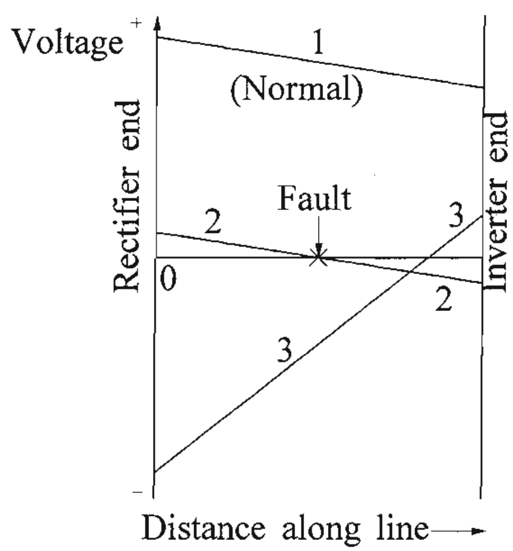


Figure 10.46 Voltage profile of a dc line:
1. Under normal operation
2. With dc line fault and normal control
3. With fast-acting line protection

Fast-acting line protection [7]

The normal control action of the converters, while limiting the fault current to I_m, does not extinguish the fault arc. Therefore, additional control is used to reduce the fault current and recovery voltage across the fault path to zero.

The fault is detected by a collapse in dc voltage usually at the rectifier and by a decrease in the current at the inverter. Both magnitude of voltage drop and rate of change of voltage may be used to detect the fault. Faults on the ac system beyond the dc link do not produce such rapid voltage changes.

To clear the fault, the inverter is kept in inversion and the rectifier is also driven to inversion. To establish terminal voltages of correct polarity for fault clearing, angle β of the inverter is given a maximum limit of about 80° (which allows the inverter voltage to run down to low value but not to reverse) and the rectifier ignition delay angle α is shifted considerably beyond 90°, to about 140°. The resulting voltage profile is as indicated by curve 3 in Figure 10.46. The current in the pole attempts to reverse direction. However, the current in the rectifier cannot reverse because of the unidirectional current characteristic of the valves. Therefore, the current is reduced to zero rapidly (in about 10 ms). This fault clearing process is called "forced retard."

DC overhead lines are restarted after allowing for de-ionization of the air surrounding the arc (60 to 200 ms). If the fault is temporary and the restart is successful, the voltage and current are ramped up. Typically, the total time for fault clearing and return to rated power transfer is on the order of 200 to 300 ms. The recovery time is higher for dc links connected to weak ac systems.

Automatic restarts are not attempted for wholly cable systems because cable faults are nearly always permanent faults.

10.7.2 Converter Faults

Most dc power circuit faults in the converter station will require either the valve group or the pole to be shut down.

A valve group fault, unless it is of a minor nature, will require the entire pole to cease transmission of power. Usually a very fast current reduction to zero is ordered. Coincidentally, the firing angle at the rectifier is shifted to at least 90° and possibly well into the inverter region. The current in the pole can be brought to zero in less than 30 ms.

An isolation sequence will follow which may take several seconds to execute, depending on the type of valve group isolators used. Then the remaining valve groups in the pole may be restarted in the normal manner.

10.7.3 AC System Faults

For ac system transient disturbances, the dc system's response is generally very much faster than that of the ac system. The dc system either rides through the disturbance with temporary reduction of power or shuts down until the ac system recovers sufficiently to allow restarting and restoration of power. Commutation failures and recovery from ac system faults represent important aspects of dc system operation.

Rectifier side ac system faults

For remote three-phase faults, the rectifier commutation voltage drops slightly. This results in a reduction of rectifier direct voltage and hence the current. The current regulator decreases α to restore current by increasing voltage. If α hits the α_{min} limit, the rectifier switches to CIA mode of control. This transfers current control to the inverter whose current order is less than that of the rectifier by an amount equal to the current margin (I_m). If the low voltage persists, the tap changers will operate to restore the direct voltage and current to normal. Depending on how low the voltage drops, the VDCOL may regulate current and power transfers. For close-in three-phase faults, the rectifier commutation voltage drops significantly. The dc system shuts down under VDCOL control until the fault is cleared.

In theory, dc power may be transferred at very low rectifier voltages. This would require the inverter to assume current control by lowering its voltage and greatly increasing β. The resulting increased consumption of reactive power may be more detrimental to the ac system performance than briefly shutting down the dc system.

Remote single-phase and phase-to-phase faults do not usually result in shutting down of the dc link. The average of the alternating voltages is higher than that for three-phase faults. If the resulting direct voltage is sufficiently high, the dc system is likely to ride through the disturbance without any noticeable effect. If, on the other hand, the reduction in direct voltage is significant, the response is similar to that for remote three-phase faults.

For close-in unbalanced faults, the harmonic ripple in the direct voltage may be higher than normal. This may produce ripples in the direct current with a large second harmonic component. The line reactors and filters, designed for smoothing out normal characteristic harmonics, are not effective in reducing the second harmonics. The high ripple current could result in current extinction. Depending on the type of valve-firing system used, this may require blocking of the dc link [7].

Inverter side ac system faults

For remote three-phase faults resulting in small voltage dips at the inverter, an increase in direct current occurs. The rectifier CC and the inverter CEA (or constant voltage) controls respond to the changes. Tap changes will occur to restore converter firing angle and direct voltage, if the low alternating voltage persists.

If the voltage dip is significant, the reduction in commutating voltages may lead to temporary commutation failure at the inverter, prior to any corrective control action. With inverter operation at a γ of 18°, it is likely that a voltage reduction by 10% to 15% will cause commutation failure. It takes about 1 or 2 cycles to clear the commutation failure. Following this, some power may be transmitted with the rectifier direct voltage reduced to match the reduction in inverter direct voltage. The resulting increase in reactive power may necessitate reduction of direct current. The VDCOL function (see Section 10.4.1) normally provided by the dc control system will cause this reduction of direct current. During extremely low voltage conditions, repeated commutation failures cannot be avoided. Therefore, it may be necessary to block and bypass the valves until the ac voltage recovers.

Unbalanced faults (both remote and close-in) may lead to commutation failure, partly due to phase shifts in the timing of the phase voltage crossings. For a severe contingency, it may be necessary to block and then restart the inverter.

When the fault has cleared, the allowable rate of restoration is dependent on the strength of the ac system. The controls are adjusted to provide the desired rate of power buildup. The performance of the overall power system following any system disturbance depends largely on the ac/dc system interaction as discussed below. It is also influenced by the subtle design features and response adjustments associated with the converter controls. These tend to vary with manufacturers. Special control strategies may be helpful in specific cases.

Recovery from ac system faults [18]

The post-fault system performance for ac system faults is far more sensitive to system parameters than for dc system faults. Recovery after an ac system fault is easier and can be more rapid with a strong ac system. Weak ac systems may have difficulty providing sufficient reactive power at the rate required for fast dc system restoration. Such systems also exhibit high temporary overvoltages and severe voltage distortion due to harmonics caused by inrushing magnetizing currents. These may cause subsequent commutation failures. Consequently the rate of recovery has to be slow.

The time for the dc system to recover to 90% of its pre-fault power is typically in the range of 100 ms to 500 ms, depending on the dc and ac system characteristics and the control strategy used. The dc system characteristics which influence the allowable rate of recovery are the line inductance and capacitance (particularly for cables), size of dc reactor, resonant harmonic frequencies of the line, converter transformer and filter characteristics. The significant ac system characteristics are ESCR, impedance at low order (2^{nd} to 4^{th}) harmonics, damping characteristics of loads near the dc system, system inertia, and method of voltage control near the converter bus.

Control strategies that assist in satisfactory dc system recovery (without post-fault commutation failures) include delayed or slow ramp recovery, and at reduced current level during recovery.

The VDCOL function can play a significant role in determining the recovery from faults. It limits the current order as a function of either the direct voltage or the alternating voltage. Consequently, reactive power demand is reduced during periods of depressed voltage. This helps prevent further deterioration of ac system voltage. Following fault clearing, the current order limit imposed by the VDCOL may be removed after a delay and gradually increased at a desired ramping rate.

From the viewpoint of ac system stability and minimization of dc power interruption, too slow a recovery is undesirable. The control strategies must therefore be tailored to meet specific needs of an application so as to maximize the recovery rate without compromising secure recovery of the dc system. Such strategies should be based on a detailed study of the individual system.

Special measures to assist recovery

Special measures may be used to assist HVDC system recovery from disturbances and to protect the valves. These measures act on either the firing angle directly or the current order. They depend on the requirements of a specific installation. The following are examples of such measures:

- Circuits that increase α_{min} from approximately 5° to over 30° during ac undervoltage conditions.
- Circuits in the inverter which transiently increase γ should γ slip below the γ_{min} limit. Then γ is increased on all succeeding firings for a prescribed period of time.
- Circuits that advance the firing angle limits by about 10° during start-up of the second valve group in a pole to prevent commutation failures.
- Circuits that increase β immediately following commutation failure so that the next valve is fired early to aid the recovery and to lessen the likelihood of subsequent commutation failure. Typically, β might be moved to 40°, 60°, and 70° on successive commutation failures. Should commutation failure cease, β would gradually retreat to its original value over a few hundred milliseconds. However, if it does not cease, a temporary bypass is usually ordered.

10.8 MULTITERMINAL HVDC SYSTEMS

In the previous sections, we considered the performance and application of point-to-point dc links, i.e., two-terminal dc systems. Successful application of such systems worldwide has led power system planners to consider the use of dc systems with more than two terminals. It is increasingly being realized that multiterminal dc (MTDC) systems may be more attractive in many cases to fully exploit the economic and technical advantages of HVDC technology.

The first MTDC system designed for continuous operation is the Sardinia-Corsica-Italy scheme. This is an expansion of the Sardinia-Italy two-terminal dc system built in 1967; a third terminal tap was added at Corsica in 1991. The two-terminal dc system between Des Cantons in Quebec and Comerford in New Hampshire built in 1986 is being extended to a three-terminal and then possibly to a five-terminal scheme [22]. Similarly, other MTDC systems are likely to evolve from the expansion of existing two-terminal schemes.

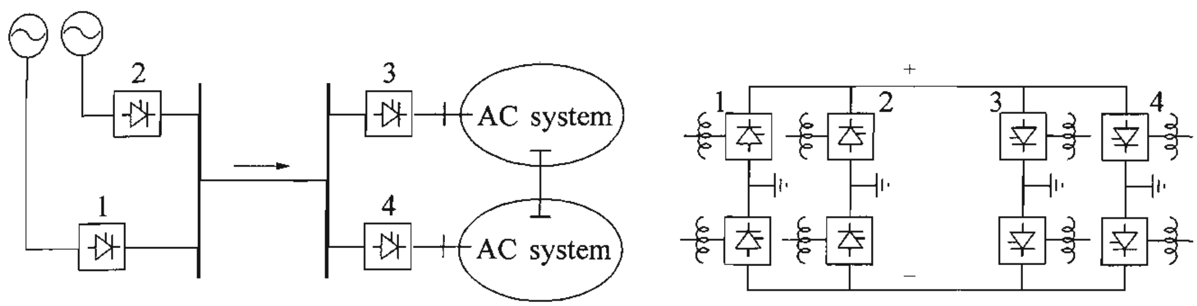
In this section, we will describe alternative MTDC system configurations and basic principles of controlling such systems. References 8, 23, 24, and 25 are recommended for further reading.

10.8.1 MTDC Network Configurations

There are two possible connection schemes for MTDC systems:

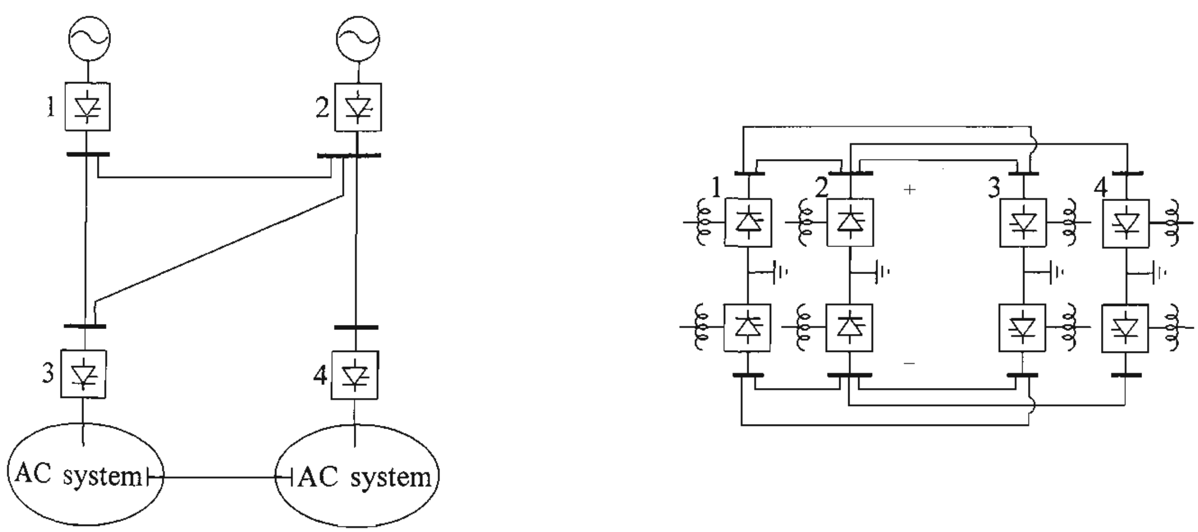
- Constant voltage parallel scheme
- Constant current series scheme

In the parallel scheme, the converters are connected in parallel and operate at a common voltage. The connections can be either radial or mesh. Figures 10.47 and 10.48 depict the two types of connections.



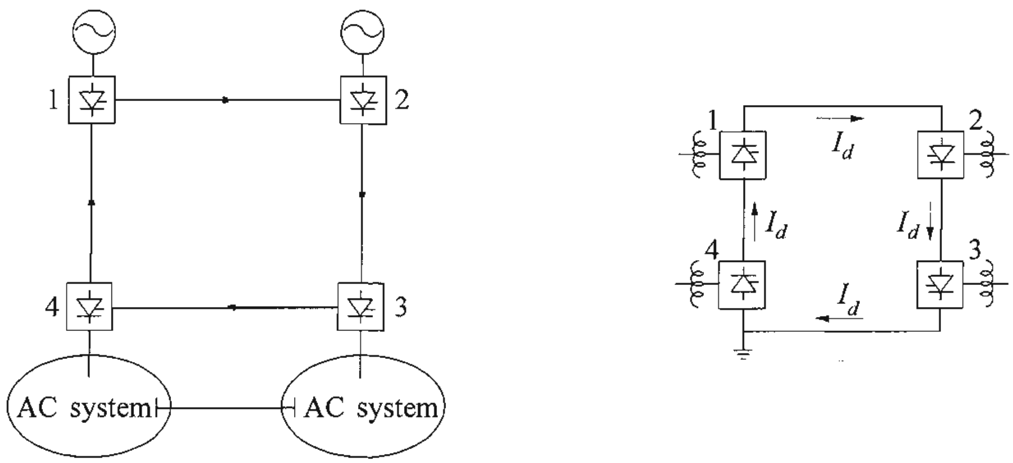
(a) System diagram (b) Converter stations' connection

Figure 10.47 Parallel MTDC bipolar scheme with radial dc network



(a) System diagram (b) Converter stations' connection

Figure 10.48 Parallel MTDC bipolar scheme with mesh type connection



(a) System diagram (b) Converter stations' connection

Figure 10.49 Series MTDC scheme

In the series scheme, the converters are connected in series with a common direct current flowing through all terminals. The dc line is grounded at one location. Figure 10.49 illustrates the series connection.

It is also conceivable to have a hybrid MTDC system involving both series and parallel-connected converter stations. The availability of dc circuit breakers [25] will add to the flexibility of MTDC systems and influence their selection.

The majority of studies and proposed applications of MTDC have considered parallel configuration with radial-type connection. The mesh connection, although offering more redundancy, requires greater length of dc lines.

Consideration of series connected schemes has been generally confined to applications with small power taps (less than 20%) where it may be more economical to operate at a higher current and lower voltage than for a full voltage tap at full voltage and reduced current. In a series tap, the voltage rating is proportional to the power capacity of the tap. However, the converter transformer must have full dc network voltage insulation. Flexibility of the power transfer could require a wide range for the transformer taps of the series stations.

In any specific MTDC system application, its special needs will determine the preferred network configuration. In general, the parallel scheme is widely accepted as the most practical scheme with fewest operational problems. Compared to the series-connected scheme, it results in fewer line losses, is easier to control, and offers more flexibility for future extension.

10.8.2 Control of MTDC Systems

The basic control principle for MTDC systems is a generalization of that for two-terminal systems. The control characteristic for each converter is composed of segments representing constant-current control and constant-firing angle control (CEA for inverter and CIA for rectifier). In addition, an optional constant-voltage segment may be included.

The converter characteristics, together with the dc network conditions, establish the operating point of the system. For a common point to exist, converter control characteristics must intersect.

For MTDC systems, there is considerable room for providing flexibility of options to meet the requirements of individual systems. References 23 and 25 discuss different proposed control strategies.

The following is a general discussion of significant aspects related to control of parallel- and series-connected systems.

Parallel-connected systems

In a parallel-connected system, one of the terminals establishes the operating voltage of the dc system, and all other terminals operate on constant-current (CC) control. The voltage setting terminal is the one with the smallest ceiling voltage. This may be either a rectifier on CIA control or an inverter on CEA control.

The *V-I* characteristics for a four-terminal dc system are shown in Figure 10.50. The individual converter characteristics are shown in Figure 10.50(a), and the combined characteristics are shown in Figure 10.50(b). It is assumed that two of the terminals are operating as rectifiers and the other two terminals as inverters. The characteristics shown are for one pole. For the sake of simplicity, VDCOLs are not shown. It is assumed that each terminal has only two modes of control (CC, and CEA or CIA); the voltage control option is not considered.

In Figure 10.50, it is assumed that rectifier 1 is the voltage-setting terminal (CIA mode). Tap changers keep angles within the desired range. To maintain stable control operation, a positive-current margin must be maintained.

If an inverter is the voltage-controlling station, it is vulnerable to inadvertent overloading. It is unable to control the current at its terminals in the event of a system disturbance or load change. Disconnection of a current-controlled inverter will require reallocation of rectifier current settings to prevent overloading the voltage-controlled inverter.

On the other hand, if a rectifier defines the system voltage, the operation is more stable. All inverters control current, thereby avoiding operation in the less stable CEA control mode. The voltage-controlling rectifier is capable of protecting itself without causing overloading of other stations. The system is less dependent on high-speed communication and hence is more secure. In general, voltage control at a large rectifier terminal should provide better performance.

The following are the main drawbacks of parallel-connected MTDC systems:

- Any disturbance on the dc system (line fault or commutation failure) affects the entire dc system.
- Reversal of power at any terminal requires mechanical switch operation.

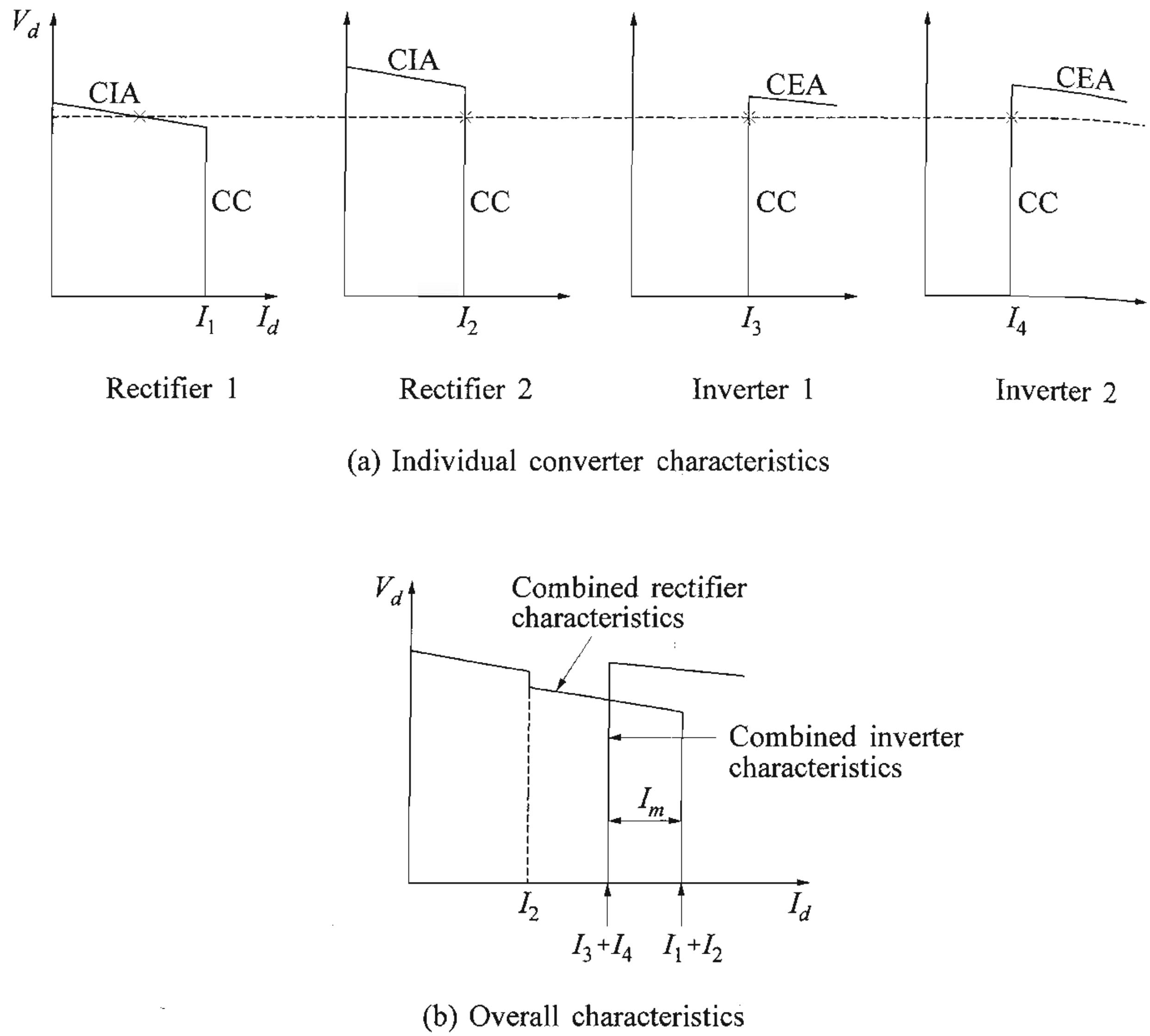


Figure 10.50 Control characteristics of parallel-connected MTDC systems

- Blocking of a single bridge, in a converter station consisting of two or more series-connected bridges, requires either operation of the whole system at reduced voltage or disconnection of the affected station.

- Commutation failure at an inverter can draw current from other terminals and this may affect recovery.

Series-connected systems

In a series-connected system, current is controlled by one terminal, and all other terminals either operate at constant-angle (α or γ) control or regulate voltage. Figure 10.51 illustrates the control strategy usually considered for series systems.

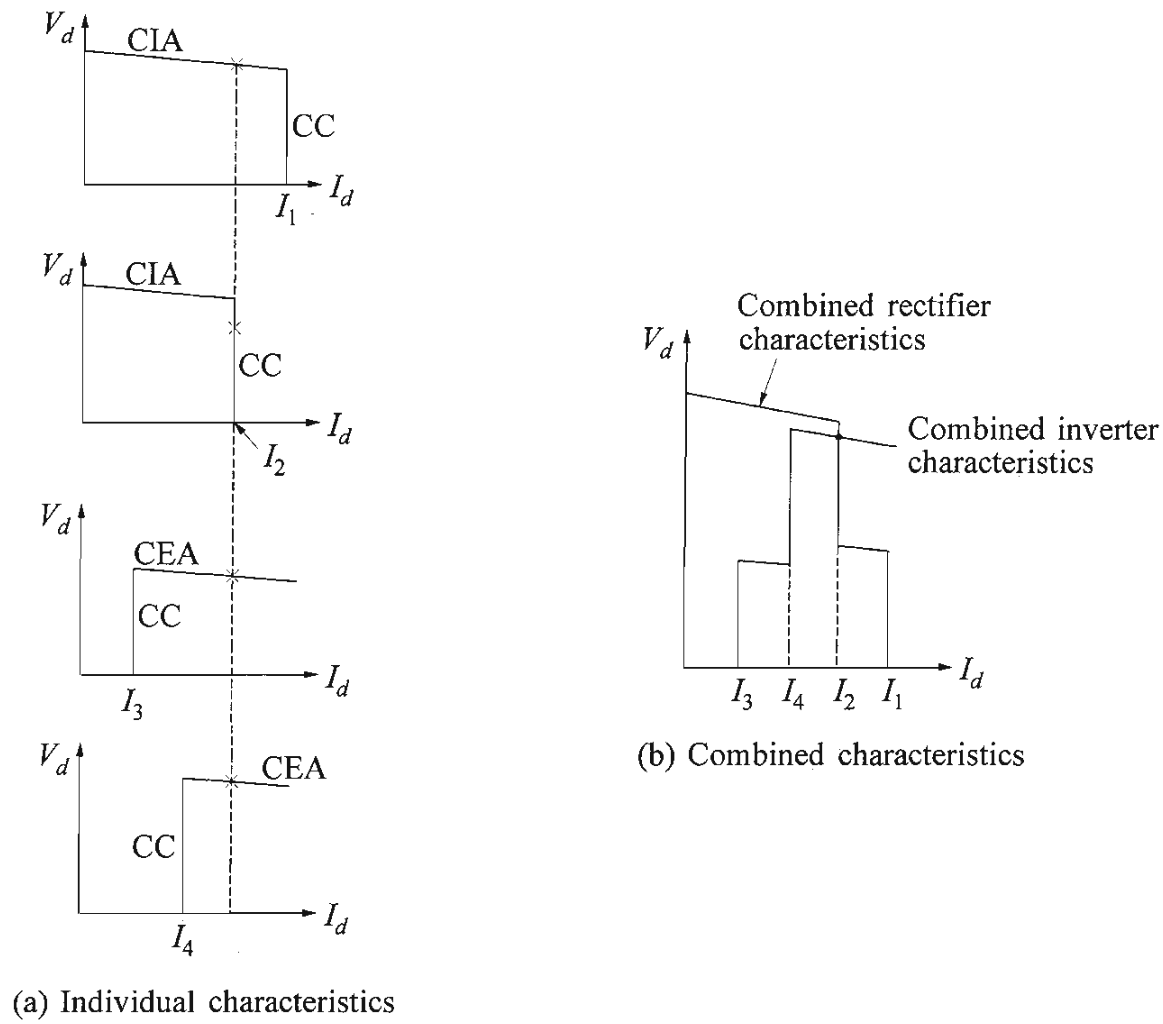


Figure 10.51 Control characteristics of series systems

Current control is assumed by a rectifier if the sum of the rectifier voltages at the ordered current is greater than the sum of the inverter voltages; the rectifier with the lowest current order assumes the current control. On the other hand, if the sum of the inverter voltages is greater, the inverter with higher current order assumes current control.

For series systems, the voltage references must be balanced, whereas for parallel systems current references must be coordinated. However, for series systems the coordination problem is not as critical as it could be with parallel systems.

The series systems allow high-speed reversal of power at any terminal without the need for switching operations. Bridges and terminals can be taken out of service without affecting the rest of the system. Communication between terminals is required for controlling line loadings to minimize losses; this can be achieved with a relatively slow communication.

The operation of converters in series requires converter operation with high firing angles. This can be minimized by tap-changer control and backing off one bridge against another.

The following are the main drawbacks of the series-connected systems:

- As the voltage to ground is different in various parts of the system, insulation coordination is complex and expensive. Losses are higher in portions with lower voltage.
- A permanent line fault causes interruption of the entire system.
- Flexibility for future extension is limited.

10.9 MODELLING OF HVDC SYSTEMS

In this section, we will discuss the modelling of HVDC systems in power-flow and stability studies. The representation of the dc systems requires consideration of the following:

- Converter model
- DC transmission line/network model
- Interface between ac and dc systems
- DC system controls model

The representation of the converters is based on the following basic assumptions:

(a) The direct current I_d is ripple-free.

(b) The ac systems at the inverter and the rectifier consist of perfectly sinusoidal, constant frequency, balanced voltage sources behind balanced impedances. This assumes that all harmonic currents and voltages introduced by the commutation system do not propagate into the ac system because of filtering.

(c) The converter transformers do not saturate.

The validity of making the first two assumptions for power-flow and stability studies has been demonstrated in reference 27.

10.9.1 Representation for Power-Flow Solution

From the analysis presented in Section 10.2, the converter equations may be summarized as follows:

$$V_{do} = \frac{3\sqrt{2}}{\pi}BTE_{ac}$$

$$V_d = V_{do}\cos\alpha - \frac{3}{\pi}X_c I_d B$$

or

$$V_d = V_{do}\cos\gamma - \frac{3}{\pi}X_c I_d B$$

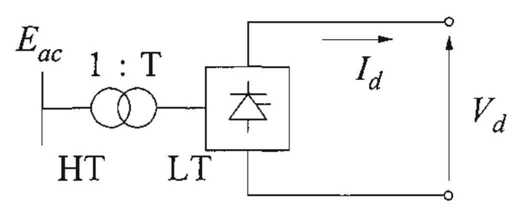
$$\phi \approx \cos^{-1}(V_d/V_{do}) \qquad (10.45)$$

$$P = V_d I_d = P_{ac}$$

$$Q = P\tan\phi$$

where

E_{ac} = RMS line-to-line voltage on HT bus
T = transformer turns ratio
B = no. of bridges in series
P = active power
Q = reactive power
X_c = ωL_c = commutating reactance per bridge/phase
V_d, I_d = direct voltage and current per pole



The equation used above for determining the power factor angle (ϕ) is approximate. It simplifies analysis significantly and gives results of acceptable accuracy, consistent with the level of accuracy associated with iterative solution techniques used for power-flow analysis. For specific applications requiring greater accuracy, exact relationships between ac and dc quantities derived in Section 10.2.2 may be used.

For the purpose of illustration, we will consider a two-terminal dc link. Using the subscripts r and i to denote rectifier and inverter quantities, respectively, the equation for a dc line having a resistance R_L is given by

$$V_{dr} = V_{di} + R_L I_d \qquad (10.46)$$

(a) AC/DC interface at the HT bus

Power-flow analysis requires joint solution of the dc and ac system equations. One approach is to solve the two sets of equations iteratively, as illustrated in Figure 10.52, with the converter transformer HT bus (ac side) providing the interface between the ac and dc equations.

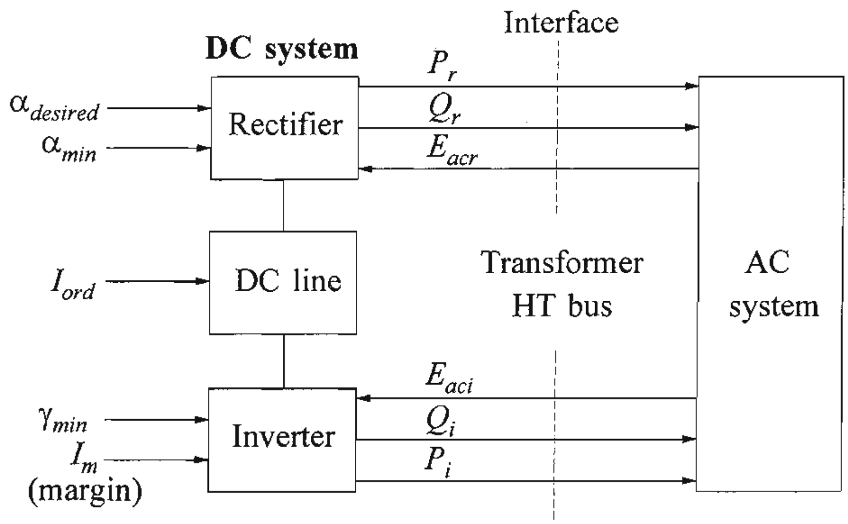


Figure 10.52

Here E_{acr} and E_{aci} are considered to be input quantities for the solution of dc system equations. They are known from the previous step in ac solution.

Variables P_r, Q_r, P_i and Q_i are considered to be the outputs from the solution of the dc system equations. They are used in the next iteration for solving the ac system equations.

The dependent and independent variables in the solution of dc equations depend on rectifier and inverter control modes. The three possible modes of operation are:

Mode 1: Rectifier on CC control; inverter on CEA control
Mode 2: Inverter on CC control; rectifier on CIA control
Mode 3: Rectifier on CIA control; inverter on modified characteristic

In mode 1, alternative inverter control functions are constant voltage control and constant-β control (see Section 10.4.1). For purposes of illustration we will consider here only the CEA control mode.

(1) Mode 1: rectifier on CC control and inverter on CEA control:

In mode 1, we have

- Inverter firing angle adjusted to give $\gamma = \gamma_{min}$.
- Rectifier firing angle adjusted to give $I_d = I_{ord}$.
- Rectifier transformer tap adjusted to give α within a desired range.
- Inverter transformer tap adjusted to give desired voltage.

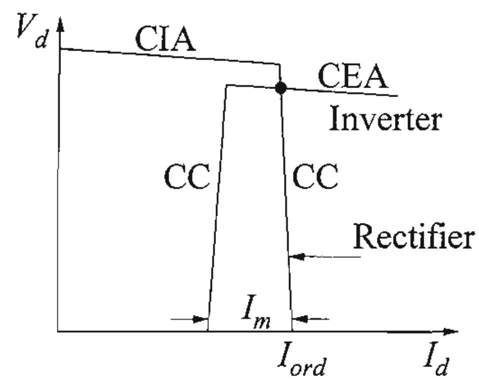


Figure 10.53

From Equation 10.45, with $I_d = I_{ord}$, we may write inverter equations as follows:

$$V_{doi} = \frac{3\sqrt{2}}{\pi} B_i T_i E_{aci}$$

$$V_{di} = V_{doi}(\cos\gamma_{min}) - \frac{3}{\pi} X_{ci} B_i I_{ord} \tag{10.47}$$

$$\phi_i = \cos^{-1}(V_{di}/V_{doi})$$

$$P_i = V_{di} I_{ord}$$

$$Q_i = P_i \tan\phi_i$$

Since γ_{min} and I_{ord} are known and E_{aci} is given by the previous ac solution, V_{di}, P_i and Q_i can be computed. The transformer tap can be adjusted to give V_{di} within the desired range.

The rectifier equations are

$$V_{dr} = V_{di} + R_L I_{ord}$$

$$V_{dor} = \frac{3\sqrt{2}}{\pi} E_{acr} B_r T_r \tag{10.48}$$

$$\alpha = \cos^{-1}\left(\frac{V_{dr}}{V_{dor}} + \frac{X_{cr} I_{ord}}{\sqrt{2} E_{acr} T_r}\right)$$

In the above equations voltage E_{acr} is known from the previous ac solution. The turns ratio T_r is adjusted to give α within the desired range.

$$\begin{aligned} \phi_r &= \cos^{-1}(V_{dr}/V_{dor}) \\ P_r &= V_{dr}I_{ord} \\ Q_r &= P_r \tan\phi_r \end{aligned} \tag{10.49}$$

Here P_i, P_r, Q_i and Q_r are outputs to be used in the next iteration of the ac solution.

(2) Mode 2: inverter on CC control and rectifier on CIA control

In mode 2, we have

- Rectifier firing angle $\alpha = \alpha_{min}$.
- Inverter firing angle adjusted to give $I_d = I_{ord} - I_m$.
- Rectifier transformer tap adjusted to maximize dc voltage.
- Inverter transformer tap adjusted so that $\gamma > \gamma_{min}$ and var consumption is minimized.

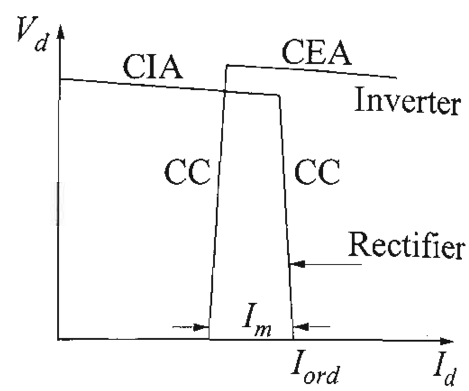


Figure 10.54

With $I_d = I_{ord} - I_m$, the rectifier equations are

$$\begin{aligned} V_{dor} &= \frac{3\sqrt{2}}{\pi} B_r T_r E_{acr} \\ V_{dr} &= V_{dor}\cos\alpha_{min} - \frac{3}{\pi} X_{cr}(I_{ord} - I_m) B_r \\ \phi_r &= \cos^{-1}(V_{dr}/V_{dor}) \\ P_r &= V_{dr}(I_{ord} - I_m) \\ Q_r &= P_r \tan\phi_r \end{aligned} \tag{10.50}$$

In the above equations, E_{acr} is known from the previous ac solution, and I_d is held at $I_{ord} - I_m$ by the inverter. Turns ratio T_r may be adjusted to maximize V_{dr}.

With E_{aci} known from the ac solution, the inverter equations may be solved as follows:

$$\begin{aligned} V_{doi} &= \frac{3\sqrt{2}}{\pi} E_{aci} B_i T_i \\ V_{di} &= V_{dr} - R_L I_d \\ &= V_{dr} - R_L (I_{ord} - I_m) \\ \gamma &= \cos^{-1}\left[\frac{V_{di}}{V_{doi}} + \frac{X_{ci}(I_{ord} - I_m)}{\sqrt{2}E_{aci}T_i}\right] \\ \phi_i &= \cos^{-1}(V_{di}/V_{doi}) \\ P_i &= V_{di} I_d = V_{di}(I_{ord} - I_m) \\ Q_i &= P_i \tan\phi_i \end{aligned} \tag{10.51}$$

Turns ratio T_i may be adjusted to ensure $\gamma > \gamma_{min}$ and minimize var consumption. Variables P_r, P_i, Q_r and Q_i are outputs of the above calculations to be used for the next iteration of the ac solution.

(3) Mode 3: rectifier on CIA control and inverter on modified characteristic

For power-flow studies, it is usually sufficient to consider modes 1 and 2. However, for power-flow solutions (solution of network algebraic equations) associated with stability studies, it is necessary to consider the transition between modes 1 and 2. For reasons given in Section 10.4.1, the inverter characteristic is modified as shown in Figure 10.55. The segment JK, with a positive slope, provides a more stable control mode than the segment FK. One method of realizing this modified characteristic is to operate the inverter in the constant-β mode.

In mode 3, we have

- Rectifier ignition delay angle = α_{min}.
- Inverter ignition advance angle = β_c.
- $I_d = I'_d$ such that $I_{ord} > I'_d > (I_{ord} - I_m)$.

The dc system equations are solved as follows to compute the line current.

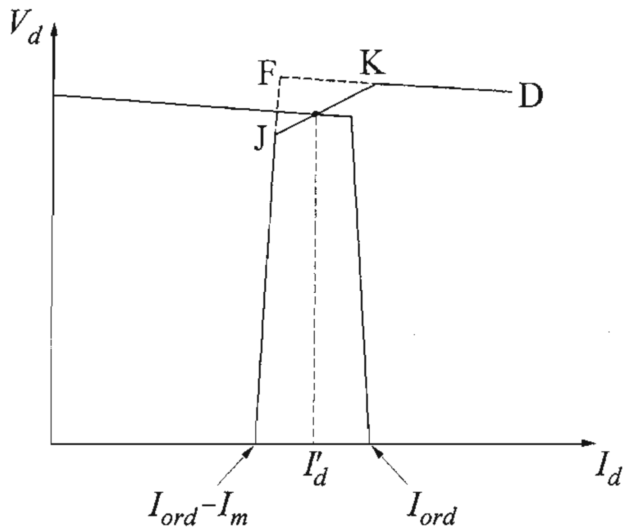


Figure 10.55

$$V_{dor} = \frac{3\sqrt{2}}{\pi} B_r T_r E_{acr}$$
$$V_{doi} = \frac{3\sqrt{2}}{\pi} B_i T_i E_{aci} \tag{10.52A}$$

Variables E_{acr} and E_{aci} are known from the previous ac solution.

$$V_{dr} = V_{dor} \cos\alpha_{min} - \frac{3}{\pi} I'_d X_{cr} B_r$$
$$V_{di} = V_{doi} \cos\beta_c + \frac{3}{\pi} I'_d X_{ci} B_i \tag{10.52B}$$

From line equation, we have

$$V_{dr} = V_{di} + R_L I'_d$$

Hence,

$$I'_d = \frac{V_{dr} - V_{di}}{R_L}$$
$$= \frac{1}{R_L}\left[V_{dor}\cos\alpha_{min} - V_{doi}\cos\beta_c - \frac{3}{\pi} I'_d (X_{cr}B_r + X_{ci}B_i)\right]$$

Rearranging, we have the following expression for I_d' in terms of V_{dor}, V_{doi}, α_{min} and β_c, whose values are known.

$$I_d' = \frac{V_{dor}\cos\alpha_{min} - V_{doi}\cos\beta_c}{R_L + \frac{3}{\pi}X_{cr}B_r + \frac{3}{\pi}X_{ci}B_i} \tag{10.53}$$

With the value of I_d' known, V_{dr} and V_{di} are calculated by using Equation 10.52B. The ac quantities can then be calculated as follows:

$$\begin{aligned}
\phi_r &= \cos^{-1}(V_{dr}/V_{dor}) \\
\phi_i &= \cos^{-1}(V_{di}/V_{doi}) \\
P_r &= V_{dr}I_d' , \quad Q_r = P_r\tan\phi_r \\
P_i &= V_{di}I_d' , \quad Q_i = P_i\tan\phi_i
\end{aligned} \tag{10.54}$$

For transient stability simulations, the tap-changer action is too slow and hence not considered.

For any given system condition, the rectifier and inverter modes of operation may not be known prior to the solution of system equations. Therefore, the following procedure may be used to establish operating modes and solve the ac and dc equations.

1. Solve for ac equations; output E_{acr}, E_{aci}.

2. (a) Solve mode 1 dc equations.
   If $\alpha > \alpha_{min}$, mode 1 condition is satisfied; go to step 3.

   (b) If $\alpha \leq \alpha_{min}$, solve for mode 2 dc equations.
   If $\gamma > \gamma_{min}$, mode 2 condition is satisfied; go to step 3.

   (c) If $\gamma \leq \gamma_{min}$, solve for mode 3 equations.

3. Calculate P_i, Q_i, P_r and Q_r. If mismatch is greater than tolerance, go back to step 1 and solve ac equations.

4. If mismatch is less than tolerance, solution is complete.

(b) AC/DC interface at the LT bus

In the representation discussed above, the ac/dc interface is at the HT side of the commutating transformer. An alternative representation is to have the ac/dc interface at the LT side (the valve side) of the commutating transformer.

An advantage of using the ac/dc interface at the LT bus is that it allows the commutation reactance to be different from the leakage reactance of the commutating transformer. Ideally, it should be the leakage reactance plus the equivalent system reactance at the HT bus. In most cases, the system reactance is small compared to the transformer reactance and, therefore, the LT bus representation may not be essential. In weak systems, this may not be true and the flexibility offered by the so-called LT representation is useful. The LT bus representation also offers flexibility in modelling SVCs, synchronous condensers, and filters connected to the tertiary winding of the converter transformers.

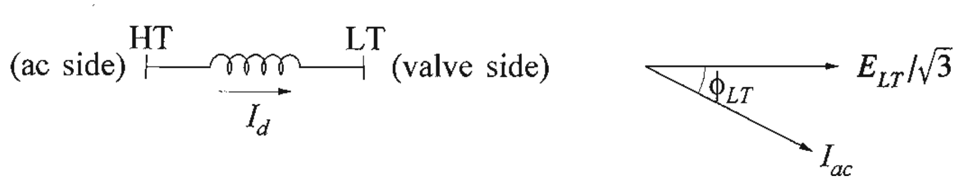
In the LT bus interface approach, the ac system representation includes converter transformers, and the ac solution includes computation of LT bus voltages. The LT voltages are used as input to the solution of dc equations. The HT bus voltage (or more precisely the commutating voltage) is computed from the LT voltage, and used in the solution of dc equations, which are essentially the same as those for the HT bus interface approach. The output of the solution of dc equations, for use in the next iteration of ac solution, is P and Q at the LT bus.

The following are the details of the calculations. Since an equivalent HT bus is used, there is no need for a transformer tap ratio in the dc equations.

Calculation of equivalent HT bus line voltage:

Let

E_{LT} = RMS line-to-line voltage at LT bus
E_{ac} = RMS line-to-line voltage behind X_c
X_c = equivalent commutating reactance per phase
ϕ_{LT} = angle between LT bus phase voltage and line current



Using the LT bus line-to-neutral voltage ($E_{LT}/\sqrt{3}$) as reference phasor, we have

$$\frac{E_{ac}}{\sqrt{3}} = \frac{E_{LT}}{\sqrt{3}} + j\frac{X_c}{B}I_{ac}(\cos\phi_{LT} - j\sin\phi_{LT})$$

$$E_{ac} = E_{LT} + j\sqrt{3}\frac{X_c}{B}\frac{\sqrt{6}I_d B}{\pi}(\cos\phi_{LT} - j\sin\phi_{LT}) \tag{10.55}$$

$$= \left(E_{LT} + \frac{6X_c}{\sqrt{2}\pi}I_d\sin\phi_{LT}\right) + j\frac{6X_c}{\sqrt{2}\pi}I_d\cos\phi_{LT}$$

Calculation of reactive power at the LT bus:

As before, active power is

$$P = V_d I_d = P_{ac}$$

and the reactive power at the equivalent HT bus is

$$Q_{HT} = P\tan\phi_{HT}$$

where

$$\phi_{HT} = \cos^{-1}(V_d/V_{do})$$

To find the reactive power at the LT bus, Q_{HT} is reduced by the three-phase $X_c I^2$ loss. Since there are B bridges in parallel,

$$Q_{LT} = Q_{HT} - 3\frac{X_c}{B}I_{ac}^2$$

$$= Q_{HT} - 3\frac{X_c}{B}\left(\frac{\sqrt{6}}{\pi}I_d B\right)^2 \tag{10.56}$$

$$= Q_{HT} - BX_c\frac{18}{\pi^2}I_d^2$$

Reference 28 uses the above approach.

Inclusion of converter station losses

The dc system equations used so far did not consider converter station losses. There are several losses associated with a converter station such as those of converter transformers, filters, valves and valve auxiliaries, and smoothing reactors. The transformer copper loss may be represented by a series resistance, while other ac side losses are neglected. Inclusion of this resistance in the commutation overlap equation, however, results in considerable complexity in the converter equations; this is not usually justified.

The losses associated with the valves and their auxiliaries may be combined with the smoothing reactor and explicitly represented as equivalent series resistance (R_{eq}) on the dc side. There is also a small valve forward voltage drop (V_{drop}) due to arc drop in mercury-arc valves or forward voltage drop in thyristors. Their effects may be included by modifying the converter equations as follows:

$$V_d = V_{do}\cos\alpha - R_c I_d - R_{eq} I_d - V_{drop} \tag{10.57}$$

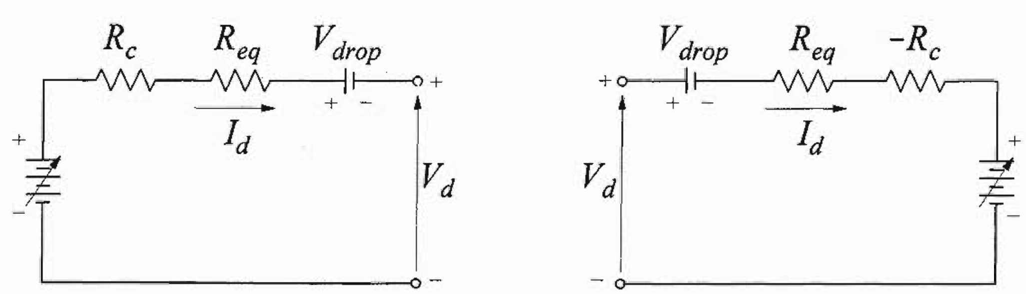
where

R_c = equivalent commutating resistance = $(3/\pi)X_c$
R_{eq} = equivalent resistance representing the losses in the valves and auxiliaries
V_{drop} = voltage drop across the valve

The above equation is applicable to a rectifier as well as an inverter. However, for inverter calculations we prefer to write the equations in terms of γ:

$$V_d = V_{do}\cos\gamma - R_c I_d + R_{eq} I_d + V_{drop} \tag{10.58}$$

Figure 10.56 shows the corresponding equivalent circuits. These modifications to the original equations present little complexity and are easy to incorporate.



(a) Rectifier (b) Inverter

Figure 10.56 Converter equivalent circuits

The effect of neglecting losses is to introduce a small error in the computed value of active power and a relatively significant error in the value of reactive power [27]. These effects could be important for the case of back-to-back links.

Multiterminal DC systems

The formulation of power-flow equations developed above applies to two-terminal dc systems. The method can be readily extended to multiterminal systems.

Two approaches have evolved for the solution of power-flow equations. One is the sequential solution approach [29] in which the ac and dc equations are solved separately at each iteration. The other is the unified solution approach [30] in which the ac and dc systems are combined and solved as one set of equations during each iteration.

Example 10.2

Figure E10.2 shows a bipolar dc link with a rating of 1,000 MW, ±250 kV. The line resistance is 10 Ω/line. Each converter has a 12-pulse bridge with $R_c=(3/\pi)X_c=12$ Ω (6 Ω for each of the 6-pulse bridges).

The performance of the bipolar link is to be analyzed by considering it to be a monopolar link of +500 kV. The rectifier ignition delay angle limit (α_{min}) is equal to 5°. The effects of converter station losses and forward voltage drop across the valves may be neglected.

The dc link is initially operating with the rectifier on CC control with α_0=18°10′, and the inverter on CEA control with γ_0=18°10′. The current margin I_m is set at 15%, and the transformer turns ratio at each converter is 0.5. At the inverter, the dc power is 1,000 MW, and the dc voltage is 500 kV (for the equivalent monopolar link).

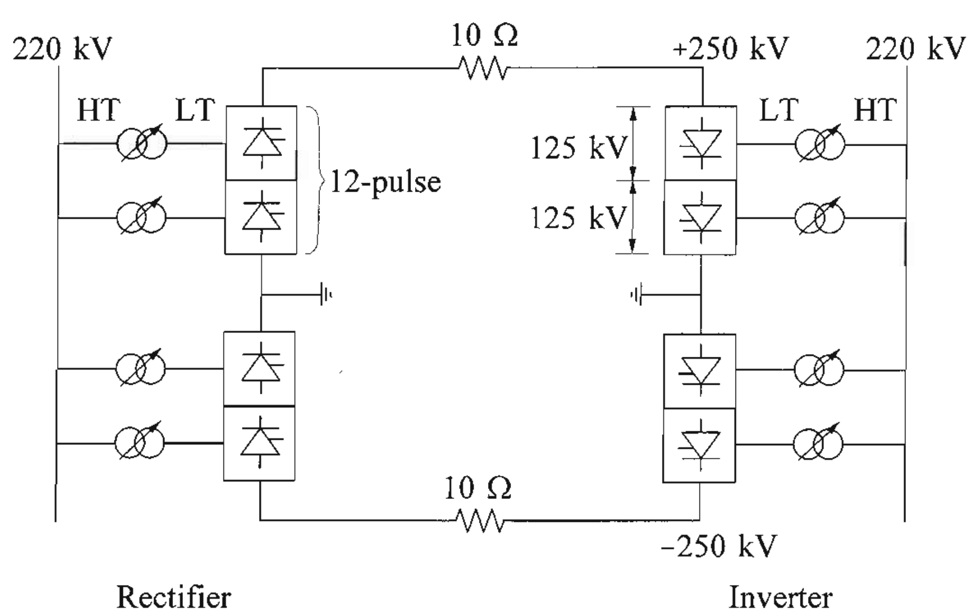


Figure E10.2

(a) For the above operating condition, compute the following:

(i) Power factor and the reactive power at the inverter HT bus.

(ii) Inverter commutation overlap angle μ.

(iii) RMS values of the line-to-line alternating voltage, fundamental component of the line current and the reactive power at rectifier HT bus.

(b) If the rectifier side HT bus ac voltage drops by 20%, compute the following:

(i) DC voltages at the rectifier and inverter terminals.

(ii) Rectifier angle α, and inverter angles γ and μ.

(iii) Active and reactive power at the inverter and rectifier HT buses.

Assume that the transformer taps have not changed and that the inverter side ac voltage is maintained constant.

(c) If the inverter side HT bus ac voltage drops by 15% and the rectifier side ac voltage remains at its initial value, determine the following after the tap changer action:

(i) The dc voltage at the rectifier and inverter terminals.

(ii) Rectifier angle α and the inverter angle γ.

(iii) Active and reactive power at the rectifier and inverter terminals.

The rectifier transformer control action attempts to hold α between 15° and 20°, and the inverter transformer control action attempts to hold the inverter dc voltage within the range of 500 to 510 kV. Assume that the maximum and minimum tap positions are 1.2 pu and 0.8 pu (corresponding to turns ratios of 0.6 and 0.4) respectively, with a tap step size of 0.01 pu.

Solution

Figure E10.3 shows the equivalent circuit of the bipolar link represented as a monopolar link of +500 kV.

(a) The initial operating condition is as follows:

$$\alpha_0 = \gamma_0 = 18.167° \qquad P_i = 1{,}000 \text{ MW}$$
$$T_r = T_i = 0.5 \qquad V_{di} = 500 \text{ kV}$$

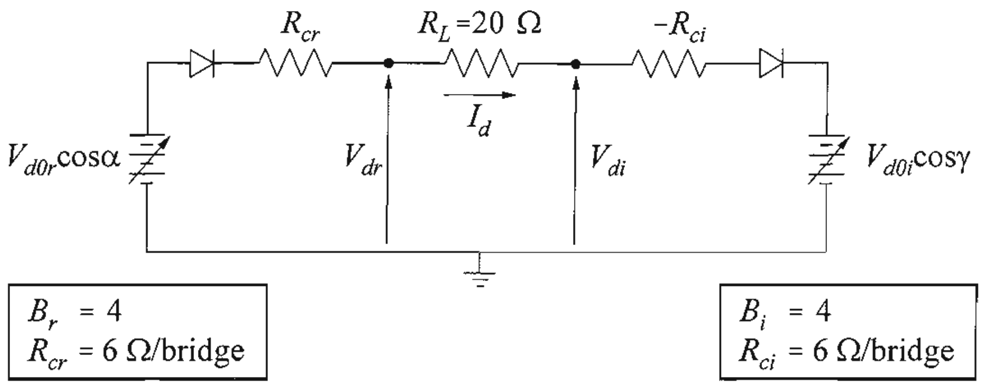


Figure E10.3 Equivalent circuit

The direct current is

$$I_d = \frac{P_i}{V_d} = \frac{1000}{500} = 2 \quad \text{kA}$$

The inverter ideal no-load voltage is

$$V_{d0i} = \frac{V_{di} + B_i R_{ci} I_d}{\cos\gamma_0}$$

$$= \frac{500 + 4 \times 6 \times 2}{\cos 18.167°}$$

$$= 576.75 \quad \text{kA}$$

(i) The power factor at the inverter HT bus is

$$\cos\phi_i \approx \frac{V_{di}}{V_{doi}} = \frac{500}{576.75} = 0.8669$$

and

$$\phi_i = 29.896°$$

The reactive power at the inverter HT bus is

$$Q_i = P_i \tan\phi_i = 1000 \tan 29.896° = 574.94 \quad \text{MVAr}$$

(ii) Since $V_{di} = V_{d0i}(\cos\gamma + \cos\beta)/2$,

$$\cos\beta = 2\frac{V_{di}}{V_{d0i}} - \cos\gamma_0$$

$$= 2\times\frac{500}{576.75} - \cos 18.167°$$

$$= 0.7837$$

and

$$\beta = 38.399°$$

Hence, the inverter commutation angle is

$$\mu_i = \beta - \gamma_0 = 38.399° - 18.167° = 20.232°$$

(iii) At the rectifier, we have

$$V_{dr} = V_{di} + R_L I_d = 500 + 2\times 20 = 540 \quad \text{kV}$$

and

$$V_{d0r} = \frac{V_{dr} + B_r R_{cr} I_d}{\cos\alpha_0}$$

$$= \frac{540 + 4\times 6\times 2}{\cos 18.167°}$$

$$= 618.85 \quad \text{kV}$$

The RMS line-to-line ac voltage at the HT bus is

$$E_{acr} = \frac{V_{dor}}{1.3505 B_r T_r}$$

$$= \frac{618.85}{1.3505\times 4\times 0.5}$$

$$= 229.12 \quad \text{kV}$$

The sum of the RMS fundamental line currents in the four transformers is

$$I_{L1r} \approx \frac{\sqrt{6}}{\pi} B_r T_r I_d$$

$$= 0.7797\times 4\times 0.5\times 2$$

$$= 3.119 \quad \text{kA}$$

The dc power at the rectifier is

$$P_r = V_{dr}I_d = 540\times 2 = 1080 \quad \text{MW}$$

The power factor at the rectifier HT bus is

$$\cos\phi_r \approx \frac{V_{dr}}{V_{d0r}} = \frac{540}{618.85} = 0.8726$$

and

$$\phi_r = 29.24°$$

The reactive power at the rectifier HT bus is

$$Q_r = P_r \tan\phi_r = 1080\tan 29.24° = 604.57 \quad \text{MVAr}$$

(b) With the transformer taps unchanged, V_{d0} is directly proportional to E_{ac}. Therefore, when the rectifier HT bus voltage drops by 20%, we have

$$V_{d0r} = 0.8\times 618.85 = 495.08 \quad \text{kV}$$

We will first assume that the dc link continues to operate in mode 1: rectifier on CC control with $I_d = I_{ord} = 2$ kA, and the inverter on CEA control with $V_{di} = 500$ kV. The corresponding direct voltage at the rectifier is

$$V_{dr} = V_{di} + R_L I_d = 500 + 20\times 2 = 540 \quad \text{kV}$$

Therefore,

$$\cos\alpha = \frac{V_{dr} + B_r R_{cr} I_d}{V_{dor}}$$

$$= \frac{540 + 4\times 6\times 2}{495.08} > 1.0$$

Therefore, mode 1 condition is not satisfied. The controls switch to mode 2: rectifier on CIA control with $\alpha = \alpha_{min} = 5°$, and the inverter on CC control with

$$I_d = I_{ord} - I_m = (1.0 - 0.15)\times 2 = 1.7 \quad \text{kA}$$

(i) The rectifier and inverter direct voltages now are

$$V_{dr} = V_{d0r}\cos\alpha - B_r R_{cr} I_d$$

$$= 495.08\cos 5° - 4\times 6\times 1.7$$

$$= 452.39 \quad \text{kV}$$

$$V_{di} = V_{dr} - R_L I_d$$
$$= 452.39 - 20 \times 1.7$$
$$= 418.39 \quad \text{kV}$$

(ii) Since the inverter ac bus voltage has not changed, V_{d0i}=576.75 kV. With I_d=1.7 kA, we have

$$\cos\gamma = \frac{V_{di} + B_i R_{ci} I_d}{V_{d0i}}$$

$$= \frac{418.39 + 4 \times 6 \times 1.7}{576.75}$$

$$= 0.796$$

and

$$\gamma = 37.23°$$

Now,

$$V_{di} = V_{d0i} \frac{\cos\gamma + \cos\beta}{2}$$

Hence,

$$\cos\beta = \frac{2V_{di}}{V_{d0i}} - \cos\gamma$$

$$= \frac{2 \times 418.39}{576.75} - 0.796$$

$$= 0.655$$

and

$$\beta = 49.10°$$

The inverter commutation angle is

$$\mu_i = \beta - \gamma = 49.10° - 37.23° = 11.87°$$

(iii) The dc power at the inverter is

$$P_i = V_{di} I_d = 418.39 \times 1.7 = 711.26 \quad \text{MW}$$

The power factor at the inverter HT bus is

$$\cos\phi_i \approx \frac{V_{di}}{V_{d0i}} = \frac{418.39}{576.75} = 0.725$$

and

$$\phi_i = 43.49°$$

The reactive power at the inverter HT bus is

$$Q_i = P_i \tan\phi_i = 711.26\tan 43.49° = 674.85 \quad \text{MVAr}$$

The dc power at the rectifier is

$$P_r = V_{dr} I_d = 452.39 \times 1.7 = 769.06 \quad \text{MW}$$

The power factor at the rectifier HT bus is

$$\cos\phi_r \approx \frac{V_{dr}}{V_{d0r}} = \frac{452.39}{495.08} = 0.914$$

and

$$\phi_r = 23.97°$$

The reactive power at the rectifier HT bus is

$$Q_r = P_r \tan\phi_r = 769.06\tan 23.97° = 341.87 \quad \text{MVAr}$$

(c) When the inverter side ac voltage drops by 15% and the rectifier voltage remains at its normal value, mode 1 operation is possible. Hence, the rectifier is on CC control with

$$I_d = I_{ord} = 2 \quad \text{kA}$$

and the inverter is on CEA control with

$$\gamma = 18.167°$$

Due to the reduction in ac voltage, the inverter dc voltage drops. The rectifier α increases and the dc voltage decreases so that I_d is maintained constant. The rectifier transformer tap changer acts to hold α between 15° and 20°, and the inverter transformer tap changer acts to hold V_{di} between 500 kV and 510 kV.

The ideal no-load voltage of a converter is directly proportional to the ac voltage and the transformer turns ratio. In (a), we computed the rectifier and inverter ideal no-load voltages under normal ac voltages and 1.0 pu tap position (turns ratio of 0.5) to be

$$V_{d0r} = 618.85 \quad \text{kV}$$

and

$$V_{d0i} = 576.75 \quad \text{kV}$$

With normal ac voltage and tap changer action, for the rectifier, we have

$$V_{d0r} = 618.85 T_r'$$

where T_r' is the pu tap position.

Similarly, for the inverter with ac voltage reduced by 15%, we have

$$V_{d0i} = 576.75(0.85)T_i' = 490.24 T_i'$$

Hence, the inverter dc voltage is

$$\begin{aligned} V_{di} &= V_{d0i}\cos\gamma - B_i R_{ci} I_d \\ &= 490.24 T_i' \cos 18.167° - 4\times6\times2 \qquad \text{(E10.1)} \\ &= 465.72 T_i' - 48 \quad \text{kV} \end{aligned}$$

The rectifier direct voltage required to maintain I_d at 2 kA is

$$V_{dr} = V_{di} + R_L I_d = V_{di} + 20\times2 = V_{di} + 40 \quad \text{kV} \qquad \text{(E10.2)}$$

This should be equal to

$$\begin{aligned} V_{dr} &= V_{d0r}\cos\alpha - B_r R_{cr} I_d \\ &= 618.85 T_r' \cos\alpha - 48 \end{aligned} \qquad \text{(E10.3)}$$

From Equations E10.2 and E10.3 we have

$$\cos\alpha = \frac{V_{di} + 88}{618.85 T_r'} \qquad \text{(E10.4)}$$

Table E10.1 shows the variations in V_{di} and α as T_i' and T_r' change from their initial values to satisfy the control requirements.

Table E10.1

T_i'	T_r'	V_{di} (kV)	α (degrees)
1.0	1.0	417.7	35.2
1.01	0.99	422.4	33.6
⋮	⋮	⋮	⋮
1.07	0.93	450.3	20.7
1.08	0.93	455.0	19.4
⋮	⋮	⋮	⋮
1.10	0.93	464.3	16.3
1.11	0.93	468.9	14.6
1.12	0.94	473.6	15.1
1.13	0.95	478.3	15.6
⋮	⋮	⋮	⋮
1.17	0.98	496.9	15.3
1.18	0.99	501.5	15.8

Notes: V_{di} computed using Equation E10.1
α computed using Equation E10.4

From the table we see that the inverter tap position increases until $T_i'=1.18$ pu (corresponding to a turns ratio of 0.59) which results in a V_{di} of 501.55 kV.

The rectifier pu tap position T_r' which meets the control requirements is 0.99 (turns ratio of 0.495); the corresponding α is 15.8° and the direct voltage from Equation E10.3 is

$$V_{dr} = 618.85 \times 0.99 \times \cos 15.8° - 48 = 541.51 \quad \text{kV}$$

At the rectifier we have

$$P_r = V_{dr} I_d = 541.51 \times 2 = 1083.02 \quad \text{MW}$$

$$\cos\phi_r \approx \frac{V_{dr}}{V_{d0r}} = \frac{541.51}{618.85 \times 0.99} = 0.884$$

$$Q_r = P_r \tan\phi_r = 1083.02 \tan\phi_r = 573.2 \quad \text{MVAr}$$

At the inverter we have

$$P_i = V_{di} I_d = 501.55 \times 2 = 1003.1 \quad \text{MW}$$

$$\cos\phi_i \approx \frac{V_{di}}{V_{d0i}} = \frac{501.55}{490.24 \times 1.18} = 0.867$$

$$Q_i = P_i \tan\phi_i = 1003.1 \tan\phi_i = 576.7 \quad \text{MVAr}$$

■

10.9.2 Per Unit System for DC Quantities

A convenient per unit system for the dc quantities has the following base values:

$$\begin{aligned} V_{dc\,base} &= B\frac{3\sqrt{2}}{\pi}V_{ac\,base} = V_{do} \\ I_{dc\,base} &= I_{dc\,rated} \\ Z_{dc\,base} &= V_{dc\,base}/I_{dc\,base} \\ P_{dc\,base} &= V_{dc\,base}I_{dc\,base} \end{aligned} \tag{10.59}$$

where

B = number of bridges in series in the dc converter
$V_{ac\,base}$ = line-to-line ac base voltage referred to the LT side of the commutating transformer

If the commutating reactance per bridge expressed in ohms is X, then the per unit total commutating reactance for the B bridges in series is

$$\bar{X}_{dc} = \frac{BX}{Z_{dc\,base}} \tag{10.60}$$

Relationship between per unit quantities in the dc and ac systems

The base power and base impedance for the ac system are

$$P_{ac\ base} = \text{MVA}_{base} = \sqrt{3}\,V_{ac\ base}I_{ac\ base}$$
$$Z_{ac\ base} = V_{ac\ base}/(\sqrt{3}\,I_{ac\ base})$$

In the ac solution, the commutating reactance is represented by the parallel combination of B individual transformer reactances. The per unit value of X_c in the ac per unit system is

$$\bar{X}_{ac} = \frac{X}{BZ_{ac\,base}}$$

Therefore, the ratio of the per unit values of X_c in the two systems is

$$\begin{aligned}\frac{\bar{X}_{dc}}{\bar{X}_{ac}} &= \frac{BX}{Z_{dc\,base}} \times \frac{BZ_{ac\,base}}{X} \\ &= B^2\left(\frac{Z_{ac\,base}}{Z_{dc\,base}}\right) = B^2\left(\frac{V_{ac\,base}}{V_{dc\,base}}\right)^2 \frac{P_{dc\,base}}{P_{ac\,base}} \\ &= \left(\frac{3\sqrt{2}}{\pi}\right)^2 \frac{P_{dc\,base}}{P_{ac\,base}} \\ &= \frac{18}{\pi^2}\frac{P_{dc\,base}}{P_{ac\,base}}\end{aligned} \tag{10.61}$$

$$\begin{aligned}\frac{\bar{I}_{dc}}{\bar{I}_{ac}} &= \frac{I_{dc}}{I_{dc\,base}}\frac{I_{ac\,base}}{I_{ac}} = \frac{I_{dc}}{B\frac{\sqrt{6}}{\pi}I_{dc}}\frac{I_{ac\,base}}{I_{dc\,base}} \\ &= \frac{\pi}{B\sqrt{6}}\frac{P_{ac\,base}}{P_{dc\,base}}\frac{V_{dc\,base}}{\sqrt{3}V_{ac\,base}} = \frac{P_{ac\,base}}{P_{dc\,base}}\frac{\pi}{\sqrt{6}}\frac{B3\sqrt{2}}{B\pi\sqrt{3}} \\ &= \frac{P_{ac\,base}}{P_{dc\,base}}\end{aligned} \tag{10.62}$$

Usually, $P_{dc\,base}$ is chosen to be equal to $P_{ac\,base}$. Alternatively, $P_{dc\,base}$ may be chosen to be the nominal rating of the dc line. It is obvious that the use of the per unit system for the dc quantities offers no particular advantage. The dc quantities may in fact be handled in terms of their natural units, and many computer programs do so.

10.9.3 Representation for Stability Studies

In a stability program, the ac network equations are represented in terms of positive-sequence quantities. This imposes a fundamental limitation on the modelling of the dc systems. In particular, commutation failures cannot be accurately predicted. Commutation failure may result from a severe three-phase fault near the inverter, unbalanced faults on the inverter side ac system, or saturation of converter transformers during dynamic overvoltage conditions.

Notwithstanding the above limitation, models of various degrees of detail have been effectively used to represent dc systems in stability studies [28,31-37]. A general functional block diagram model of dc systems is shown in Figure 10.57.

Some of the early efforts to incorporate HVDC system models into stability programs used detailed representation which accounted for the dynamics of the line and the converter controls [28,31,32]. In recent years, the trend has been toward simpler models [33]. Such models are adequate for general purpose stability studies of systems in which the dc link is connected to strong parts of the ac system. However, for weak ac system applications requiring complex dc system controls and for multiterminal dc systems, detailed models are required. Therefore, the trend is reversing and the preference is to have flexible modelling capability with a wide range of detail [8,34,35,36]. The required degree of detail depends on the purpose of the study and the particular dc system.

Each dc system tends to have unique characteristics tailored to meet the specific needs of its application. Therefore, standard models of fixed structures have not been developed for representation of dc systems in stability studies. Instead, three categories of models have evolved: (a) simple model, (b) response or performance model, and (c) detailed model with flexible modelling capability.

(a) Simple models

For remote dc links, which do not have a significant impact on the results of the stability analysis, very simple models are usually adequate. The dc links may be represented as constant active and reactive power injections at the ac terminals of the converters. Where more realistic models are required, the dc link is represented by the static converter equations and functional effects of the controls. The models appear as algebraic equations and the interface between ac and dc systems is treated in a manner similar to that described for power-flow analysis in Section 10.9.1.

(b) Response models

For general purpose stability studies the dynamics of the dc line and pole controls may be neglected. The pole control action is assumed to be instantaneous and the lines are represented by their resistances.

Many of the control functions are represented in terms of their net effects, rather than actual characteristics of the hardware. The following are the features included in a typical response type model.

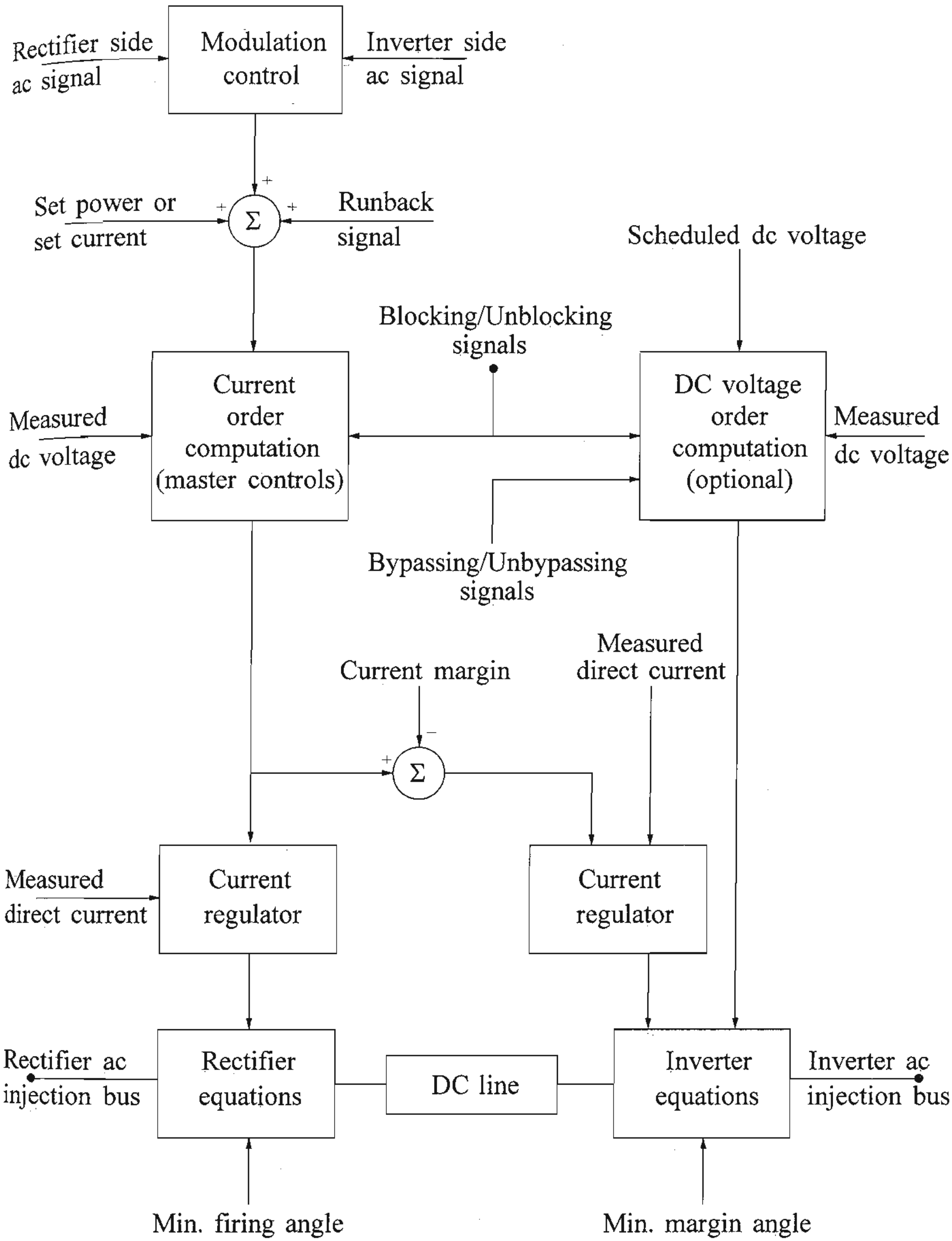


Figure 10.57 Functional block diagram of an HVDC system model

Converter and line equations:

The three modes of control, as identified before, are

- Rectifier on CC and inverter on CEA control
- Rectifier on CIA and inverter on CC control
- Rectifier on CIA and inverter on constant-β control (transition mode)

The control logic associated with the three modes of control may be incorporated into the stability solution as described in Section 10.9.1. In this case, however, transformer taps are not adjusted as they are not fast enough to be effective during the period of interest.

Current-control order with limits:

The current order is determined so as to provide either current control or power control as desired. Constraints are imposed on the current-order level to keep the current within maximum and minimum limits. The maximum current is determined by the voltage-dependent current-order limit (VDCOL) as shown in Figure 10.58. The VDCOL may be given a time delay to assist in riding through ac system faults (see Section 10.7).

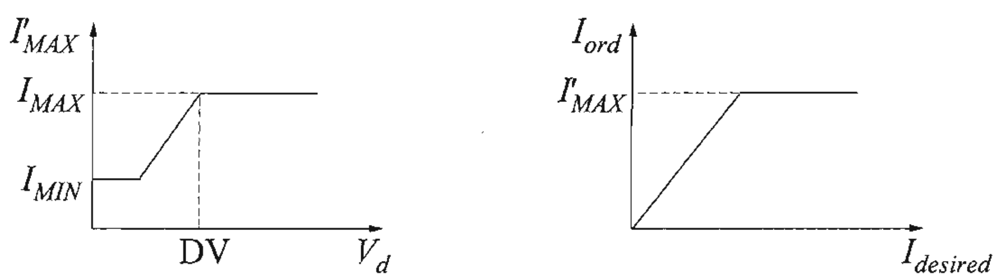


Figure 10.58 Voltage-dependent current-order limits

Control actions during ac faults:

It is necessary to have adequate representation of the actions of controls during ac faults. The following is an example of the logic that may be used to account for the control actions.

If the ac voltage on either side falls below a certain value for longer than a specified time, the direct-current order is set to zero. A ramp limit restricts the rate of decrease of direct current. The line is shut off when the current falls below a specified minimum value.

The direct line current is restored after the ac voltage recovers to an acceptable level. If the voltage recovers before the direct line current has reached its minimum value, the desired current is immediately restored to its original value. The line current increases at a specified maximum rate. If the voltage recovery occurs after the line has been shut down, the recovery is delayed by a specified time. After this, the direct line current is restored to its original value at a specified maximum rate.

The following are examples of two alternative types of recovery procedures:

(i) The current is increased by controlling rectifier α, with the inverter firing angle fixed at 90°. When the current reaches the desired value minus the current margin, the inverter extinction angle is ramped down to a specified value (normally original value) at a specified rate.

(ii) The current is increased with the maximum possible dc voltage (with $\gamma = \gamma_0$ or with $\alpha = \alpha_{min}$).

Option (i) ensures that during recovery the maximum reactive power is drawn from the ac system and may be used to control the overvoltages. Option (ii) ensures that maximum possible power is transmitted through the dc link.

The mode of operation and dc blocking and deblocking sequences are system dependent. The optimum sequence is established by experimentation.

A typical dc controller representation is shown in Figure 10.59. The dc shutoff recovery sequence for ac system faults is illustrated in Figure 10.60.

Commutation failure checks:

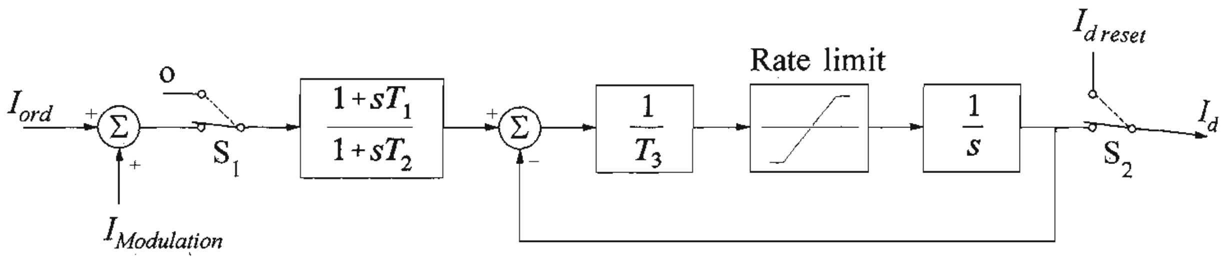
The dc model usually includes a logic for shutting off the dc line for commutation failure, detected by monitoring commutation voltage or converter margin angle.

Power/Current order modulation:

Dynamics of controls used for ac system stabilization are represented accurately, consistent with the representation used for other forms of stability controls (for example, power system stabilizers).

(c) Detailed flexible model

A wide range of dc system-modelling detail is required in stability studies. Either separate models each representing a dc link in detail or a single detailed model with facilities for simplification should be provided to achieve this flexibility. Because of the variety of controls associated with dc links, "user-defined" control models are likely to be required in addition to the basic ac/dc interface model.



Note: 1. S_1 is switched to o if $E_{acr}<E_{min\,r}$ or $E_{aci}<E_{min\,i}$ for a period $\Delta T>T_{D1}$
2. S_2 is switched to $I_{d\,reset}$ if line shuts off and E_{acr} and E_{aci} are greater than $E_{recovery}$ and $\Delta T>T_{D2}$
3. T_3 is the response time of current control loop

Figure 10.59 Current-control block diagram

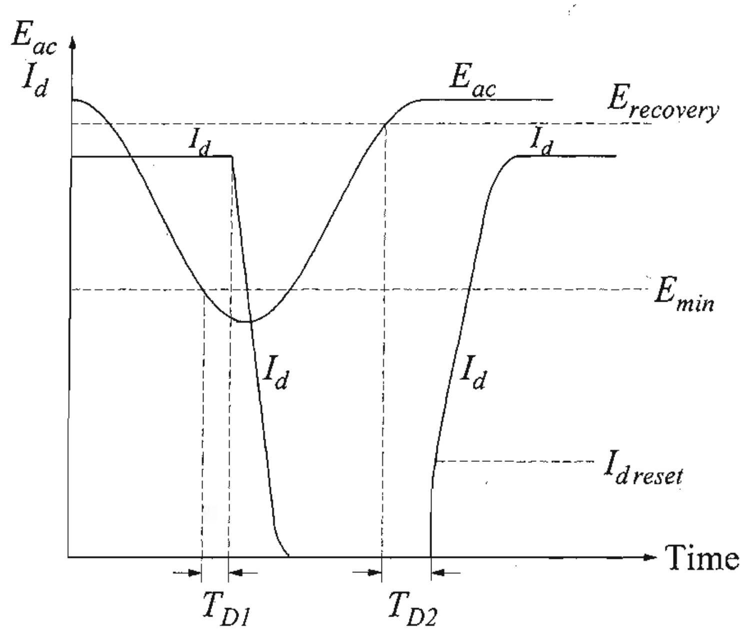


Figure 10.60 Shutoff and recovery sequence

At the highest level of detail, the following modelling features should be provided:

- DC line — a dynamic model which represents the resistance, inductive and capacitive effects of the dc line. The capacitive effects may be particularly important for cables.

- Converter controls represented by appropriate dynamic models for

- Master controls
- VDCOL including dynamics
- Current/power modulation
- Fast power change logic, including blocking/deblocking
- Pole controls capable of representing different control options such as CC, CEA, constant ac voltage, constant dc voltage, etc.
- Commutation failure simulation logic
- Special controls used to assist HVDC system recovery from disturbances, prevent commutation failure, etc.

- AC/DC interface — correct representation of the commutating voltage, commutating reactance, and transformer tertiary bus to which SVCs and synchronous condensers and other devices are connected.

In such models, the converter angle limits are embedded in the dc controls so that no special mode shift algorithm is required. However, the converter characteristics are still represented by equations relating average values of dc quantities and RMS values of ac fundamental components. This model may be referred to as "quasi steady-state model." It would accurately represent the HVDC system performance in stability studies for analysis of balanced operation, consistent with the representation used for other elements of the power system.

Since the waveforms of the voltages and currents are not represented in the model, only some general predictions regarding commutation failure can be made. These can be based on the magnitude of commutating voltage or inverter margin (extinction) angle.

A flexible quasi steady-state model should have facilities for simplifications so that models with a level of detail that is appropriate for the purpose and scope of the stability study may be used.

Detailed HVDC system models include dynamics which are usually much faster than those associated with the ac system models. In stability studies involving time-domain simulations, very small integration time steps are required to solve the dc equations. Hence, care should be exercised in integrating the ac and dc system equations. One approach often used in such situations is to solve dc equations by using time steps which are submultiples of time steps used for ac equations.

Detailed three-phase representation:

The detailed model described above, based on positive-sequence phasor representation of ac system quantities, is not accurate for analysis of unbalanced faults and for prediction of commutation failure. Accurate simulation of such conditions requires a detailed three-phase, cycle-by-cycle representation including dynamics of the ac line, filters and converter controls, during the disturbance and initial recovery. Thus, the two types of simulation, one using detailed three-phase representation of a small part of the system near the dc link and the other a single-phase quasi steady-state representation of the complete power system, are used in a complementary manner. The first type of simulation can be performed by using an electromagnetic transients program (EMTP) [38] or a dc simulator. It is conceivable that in the future this type of simulation could be incorporated into a transient stability program [6,39].

An example of detailed model

A converter control model used by some early stability programs [28, 31] with detailed representation of dc links is shown in Figure 10.61. It represents controls used for the Pacific DC Intertie and other similar systems.

In these systems, *individual phase control* is used to generate the converter firing pulses (see Section 10.4.3). This is reflected in the model. The heart of the control system is the "delay angle computer," which is represented by block 7 of Figure 10.61. It is based on Equations 10.39 and 10.40. As discussed in Section 10.4.3, the control system consists of three units: the first provides an output proportional to direct current I_d, the second provides an output proportional to $E_m \cos\gamma_c$, and the third provides an alternating voltage proportional to $E_m \cos\omega t$ [12].

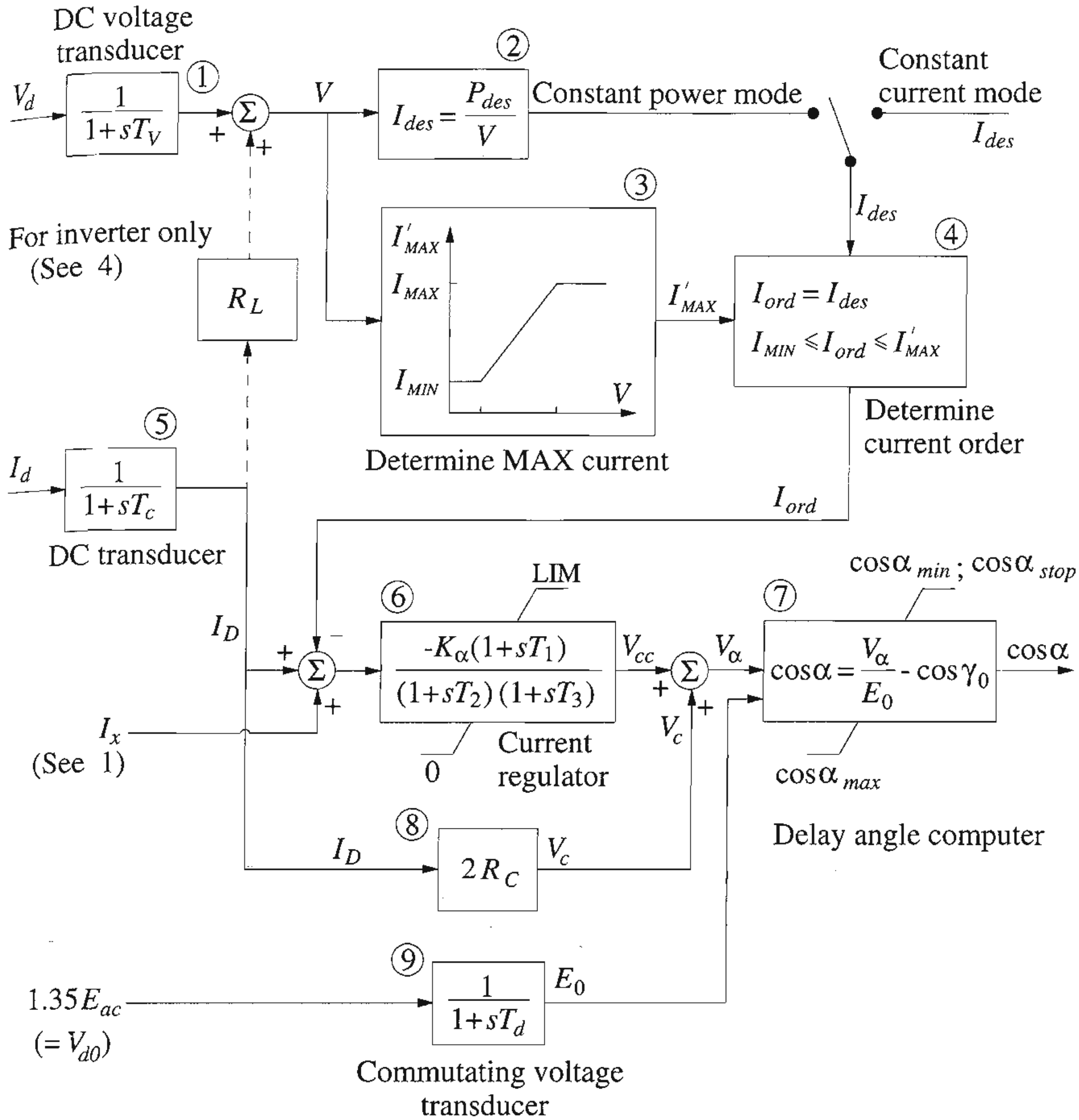
The control system uses the ac voltage to establish zero firing point reference. It then adds a direct voltage proportional to the error current to establish the proper firing point. The delay angle computer adds a bias signal $E_0 \cos\gamma_{min}$ to the ac voltage. The input E_0, the commutating voltage, in reality consists of three sinusoidal voltages, one for each pair of elements connected to an ac terminal. The output $\cos\alpha$ actually is a signal suitable for producing a firing pulse at the proper time, i.e., delayed by an angle α. The following is the basis for the "delay angle computer" block shown in Figure 10.61.

From Equation 10.39, the instant of firing $\alpha = \omega t_1$ is given by

$$\sqrt{3} E_m \cos\omega t_1 = 2 I_d X_c - \sqrt{3} E_m \cos\gamma$$

Hence,

$$\begin{aligned} \cos\alpha &= \cos\omega t_1 \\ &= \frac{2 X_c I_d}{\sqrt{3} E_m} - \cos\gamma \\ &= \frac{2 R_c I_d}{\sqrt{3} E_m} \frac{\pi}{3} - \cos\gamma \\ &= \frac{V_c}{E_0} - \cos\gamma \end{aligned} \tag{10.63}$$



Notes:

1. $I_x = I_{ref} - I_{mod}$ for rectifier; $I_x = I_{margin}$ for inverter,

   where I_{mod} is modulating signal if used, and I_{ref} is computed to give required $\cos\alpha$ under steady state.

2. Limit on current regulator output: LIM $= E_0(\cos\gamma_0 + \cos\alpha_{min}) - V_c$

3. γ_0 = initial inverter extinction angle.

4. P_{des} is specified at rectifier end. Therefore, to determine I_{ord} for inverter, the voltage drop due to line resistance has to be taken into consideration.

Figure 10.61 A detailed HVDC converter model where

$$V_c = 2R_cI_d$$
$$E_0 = \text{output of commutating voltage transducer}$$
$$= V_{d0} = \frac{3\sqrt{3}E_m}{\pi} = \frac{3\sqrt{2}E_{ac}}{\pi} = 1.35E_{ac}$$

To include current control, an additional signal V_{cc} is added so that

$$\cos\alpha = \frac{V_c}{E_0} + \frac{V_{cc}}{E_0} - \cos\gamma = \frac{V_\alpha}{E_0} - \cos\gamma \tag{10.64}$$

The upper part of Figure 10.61 shows how the current order is determined. Either constant power mode or constant current mode may be specified. The current order is limited by the maximum and minimum current limits. The maximum limit is voltage dependent (VDCOL).

There are three possible modes of operation:

- Constant ignition angle, with $\alpha = \alpha_{min}$;
- Constant current; and
- Constant extinction angle, with $\gamma = \gamma_0$.

(a) CIA mode:

The mode of operation exists when V_{cc} = LIM. The corresponding V_α is

$$V_\alpha = V_{cc} + V_c = \text{LIM} + V_c$$
$$= [E_0(\cos\gamma_0 + \cos\alpha_{min}) - V_c] + V_c$$

Hence,

$$\cos\alpha = \frac{V_\alpha}{E_0} - \cos\gamma_0 = \frac{E_0}{E_0}(\cos\gamma_0 + \cos\alpha_{min}) - \cos\gamma_0$$
$$= \cos\alpha_{min}$$

(b) CC mode:

This is the normal mode for the rectifier. In this mode V_{cc} lies between 0 and LIM. Initially I_{ref} is computed so as to give the required cosα to satisfy steady-state conditions.

(c) CEA mode:

This is the normal mode for the inverter. For this mode, V_{cc} is equal to its lower limit of zero. From Figure 10.61 and Equation 10.64, with V_{cc}=0 and $\gamma=\gamma_0$, we have

$$\cos\alpha = \frac{V_\alpha}{E_0} - \cos\gamma_0 = \frac{2R_c I_d}{E_0} - \cos\gamma_0$$

Therefore, the control will ensure that cosα corresponds to a condition with $\gamma=\gamma_0$.

Limits on the output block:

The limits ensure that the firing angle is limited to the desired values. Usually, α_{min}=5° and α_{stop}=110°.

We see that the above model reflects the dynamic performance of the converter control hardware closely. In contrast, a response model uses logic to represent many of the functions.

Chapter 17 (Section 17.2.3) gives an additional example of a dc link model with a detailed representation of pole and master controls.

Guidelines for selection of modelling detail

The modelling requirements of dc systems are influenced by the following factors:

- Nature and scope of the study,
- Type of disturbance considered, and
- Strength of the associated ac systems.

The following provide general guidelines for selection of modelling detail.

1. For studies involving disturbances remote from dc links, simple algebraic models may be used unless very low frequency interarea oscillations are excited by the fault. In such a case, response models which include the dc link

modulation controls should be used.

2. For studies associated with preliminary planning of a dc link, response models are usually adequate.

3. For studies involving dc links connected to weak ac systems, response models may be used for initial planning studies provided that they represent the relevant control action adequately. Detailed models are necessary if special dc link controls are to be studied.

4. For studies associated with planning and design specifications of equipment close to dc links, detailed models are required.

5. For studies involving multiterminal HVDC systems, detailed models are required to ensure that the coordination of the converter controls is correct. Convergence difficulties are often experienced with the use of response models for such systems. In initial studies, simple pole controls may be used to minimize the modelling requirement. Special controls necessary for multiterminal systems such as current balances must be modelled.

6. For determination of the effects of dc modulation controls, a response model is usually adequate.

7. For studies involving worst-case disturbances specified by planning/operating criteria, the modelling requirements depend on the disturbance as follows:

   (a) Bipolar outage with no restart (say, due to high-level control malfunction) or with unsuccessful restart on both poles — A simple model could be used, since the dc power would be either zero or relatively low.

   (b) Rectifier side single-line-ground ac fault with breaker and pole outage (the remaining pole would be ramped to cover the loss, subject to overload limits) — A response model is normally adequate. The zero sequence impedance of the Y-Δ converter transformer should be included in the fault shunt.

   (c) Three-phase ac faults at critical locations near the rectifier, in which case either some dc power can be transmitted during the fault, or the dc shuts down and must be restarted rapidly — The restart or recovery characteristic is important. For example, a very fast recovery could be counterproductive if the ac system is weak. Generally, a detailed model is required. In early planning stages, however, a response model including restart may be used.

(d) Inverter side single-phase ac faults which block dc power during the fault because of commutation failure — A detailed model is required since recovery time and characteristic can be critical (and multiple dc links may be affected).

(e) Various ac disturbances where dc special stability controls (modulation or fast power changes) are used — A response model is normally needed. More detailed representation of controls would be required in the case of weak ac systems. Normal power modulation can be counter-productive, and it may be necessary to model controls which decrease dc power during voltage dips (desynchronizing effect).

8. For studies involving unbalanced ac disturbances and unbalances caused by the dc system, depending on the purpose of the study, an EMTP/transient stability combination model may be desirable.

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