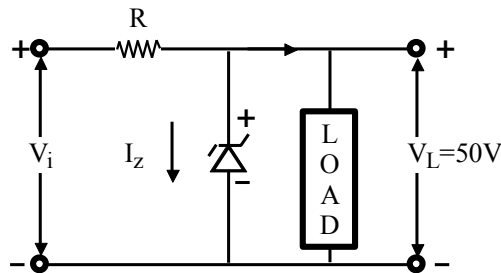


- Notes :
1. All questions carry marks as indicated.
  2. Solve Question 1 OR Questions No. 2.
  3. Solve Question 3 OR Questions No. 4.
  4. Solve Question 5 OR Questions No. 6.
  5. Solve Question 7 OR Questions No. 8.
  6. Solve Question 9 OR Questions No. 10.
  7. Solve Question 11 OR Questions No. 12.
  8. Due credit will be given to neatness and adequate dimensions.
  9. Assume suitable data whenever necessary.
  10. Illustrate your answers whenever necessary with the help of neat sketches.
  11. Use of non programmable calculator is permitted.

- 1.** a) Differentiate between Zener and avalanche breakdown. **4**
- b) Define: **4**  
 i) Transition capacitance                      ii) Diffusion capacitance
- c) The avalanche diode regulates at 50V over a diode current from 5 to 40mA. The supply voltage  $V=200V$ , calculate R to allow voltage to regulate load current  $I_L = 0$  up to  $I_{L \max}$ . What is  $I_{L(\max)}$ ? **5**

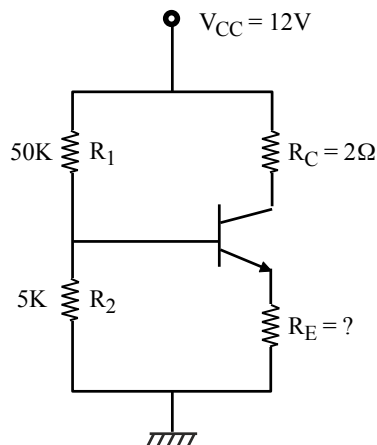


**OR**

- 2.** a) Write short note on voltage doubles. **5**
- b) Draw & explain full wave rectifier. Also derive the expression for **8**  
 i) Peak current                                      ii) Ripple Factor  
 iii) Efficiency
- 3.** a) Compare CE, CB, & CC configuration and explain why CE configuration is most useful. **5**
- b) Explain Panch trough effect in transistor. **4**
- c) Explain different operating modes of transistors. **4**

**OR**

4. a) Explain Eber-Moll model for P-N-P transistor. 6
- b) For the circuit shown in figure  $I_C = 2\text{mA}$ ,  $B \neq 00$ , calculate  $R_E$ ,  $V_{CE}$ , and stability factor 'S'. 7



5. a) Draw schematic diagram of class B push pull amp<sup>r</sup>. also show that overall efficiency of class B. Push pull amplifier is 78.5%. 5
- b) What is crossover distortion and how it can be eliminated? 5
- c) A class A power amplifier operates from  $V_{CC} = 20\text{V}$ . Draws a no signal current of 5A and feeds a load of  $40\Omega$  through step up transformer of  $N_2/N_1 = 3.16$  find 4
- i) Maximum ac signal power o/p.
  - ii) Maximum dc power input
  - iii) Efficiency.

**OR**

6. a) Explain the effect of negative feedback on bandwidth and gain of the amplifier. 7
- b) When negative feedback is applied to an amplifier of gain 100, the over all gain falls to 50. 7
- i) Calculate the fraction of the o/p voltage feedback.
  - ii) If this is maintained, calculate the value of the amplifier gain required if the overall gain is to be 75.
7. a) Explain RC phase-shift oscillator circuit. Derive the expression for frequency of oscillation. 8
- b) A crystal oscillator has the following parameter  $L = 0.33\text{H}$ ,  $C = 0.065\text{PF}$ ,  $R_m = 1\text{PF}$  &  $R = 5.5\text{K}$ . 5
- Find
- i) The series resonant frequency.
  - ii) By what percent does the parallel resonant frequency exceeds the series resonant frequency
  - iii) Find the Q factor of the crystal.

**OR**

8. a) Draw and explain the construction and working of n-channel JFET. **8**  
 b) Compare BJT and FET. **5**
9. Draw and explain the circuit of DIBO differential amplifier and derive the expression for  $I_{CQ}$ ,  $V_{CEQ}$ , differential gain  $A_d$ , input resistance and output resistance. **13**

**OR**

10. a) What is the need of level shifting circuits? Explain any one method of level shifting. **7**  
 b) Explain in brief constant current bias circuit and constant mirror circuit. **6**
11. a) State & prove De Morgan's Laws. **5**  
 b) Prove that **6**  
 i)  $\bar{y}\bar{z} + \bar{w}\bar{x}\bar{z} + \bar{w}x\bar{y}\bar{z} + w\bar{y}\bar{z} = \bar{z}$   
 ii)  $ABC + \bar{A}\bar{B}\bar{C} + \bar{A}BC + A\bar{B}\bar{C} + \bar{A}\bar{B}C + A\bar{B}C + \bar{A}BC + A\bar{B}\bar{C} = \bar{A} + \bar{B} + \bar{C}$   
 c) Explain ASCII code with example. **3**

**OR**

12. a) Perform the following. **8**  
 i)  $(337)_8 = (?)_{\text{gray}}$   
 ii)  $(45.134)_{10} = ( )_{\text{Binary}}$   
 iii)  $(2AC)_H = ( )_8$   
 iv)  $(95.73)_{10} = ( )_{\text{Excess-3}}$
- b) Give Advantage of digital system over analog system. **3**  
 c) Realize X-OR gate using NAND gate. **3**

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