

Digital & Linear Electronics Circuits

P. Pages : 2

Time : Three Hours

0773

NRT/KS/19/3365

Max. Marks : 80

- Notes :
1. All questions carry marks as indicated.
 2. Solve Question 1 OR Questions No. 2.
 3. Solve Question 3 OR Questions No. 4.
 4. Solve Question 5 OR Questions No. 6.
 5. Solve Question 7 OR Questions No. 8.
 6. Solve Question 9 OR Questions No. 10.
 7. Solve Question 11 OR Questions No. 12.
 8. Assume suitable data whenever necessary.

- 1.** a) Explain in detail the working of a two i/p TTL NAND gate with totem pole output. **6**
b) Implement the following function using 4:1 MUX. $F = m(0, 1, 2, 3, 11, 14, 15)$. **7**

OR

- 2.** a) Simplify the following logic function and realize using minimum number of NAND gates. **6**
 $F(A, B, C, D) = m(1, 2, 3, 8, 10, 11, 14) + d(7, 15)$.
b) Design a BCD to seven segment decoder from common cathode configuration. **7**
- 3.** a) Explain the working of master-slave JK Flip-Flop and explain how race around condition can be eliminated. **7**
b) Convert : **7**
1) D type Flip-Flop to JK Flip-Flop.
2) SR Flip-Flop of JK Flip-Flop.

OR

- 4.** a) Explain working of positive level triggered S.R. Flip-Flop using NAND gate. **7**
b) Write short note on ROM, EPROM, EEPROM. **7**
- 5.** a) Design full adder using two half adders. **7**
b) Explain the difference betⁿ combinational logic circuit and sequential logic circuit with suitable examples. **6**

OR

- 6.** a) Explain the working of ring counter with neat diagram and waveform. **7**
b) Explain the working of 3 bit up-down counter. **6**

